INSTITUTE OF ENGINNERING AND TECHNOLOGY LUCKNOW

(An Autonomous Constituent Institute of Dr. A.P.J. Abdul Kalam Technical University, Lucknow)

Syllabus

For

M.Tech

(MICROELECTRONICS ENGINEERING)

SCHEME OF EXAMINATION
M. Tech. (Microelectronics)

First Year:First Semester Examination

Course Code	Subject Name	Credit	Periods			Evaluation Scheme					Subject Total
						Theory			Practical		
			L	T	P	CT	TA	ESE	TA	ESE	
MTMC-101	Analog CMOS Circuit	3	3	1	0	20	10	70	-	-	100
MTMC-102	Physical Electronic	3	3	1	0	20	10	70	-	-	100
MTMC-01X	Elective - I	3	3	1	0	20	10	70	-	-	100
MTMC-02X	Elective - II	3	3	1	0	20	10	70	-	-	100
	Research Process & Methodology	3	3	1	0	20	10	70	-	-	100
MTMC-151	VLSI Circuit Design Lab	2	0	0	6	-	-	-	20	30	50
MTMC-152	Analog Signal Processing Lab	1	0	0	6	-	-	-	20	30	50
Total		**18**	**15**	**0**	**12**						**600**

SCHEME OF EXAMINATION
M. Tech. (Microelectronics)

First Year: Second Semester Examination

Course Code	Subject Name	Credit	Periods			Evaluation Scheme					Subject Total
						Theory			Practical		
			L	T	P	CT	TA	ESE	TA	ESE	
MTMC-201	VLSI Design	3	3		0	20	10	70	-	-	100
MTMC-202	VLSI Testing & Verification	3	3	1	0	20	10	50	-	-	100
MTMC-03X	Elective - III	3	3	1	0	20	10	50	-	-	100
MTMC-04X	Elective - IV	3	3	1	0	20	10	50	-	-	100
MTMC-05X	Elective - V	3	3	1	0	20	10	50	-	-	100
MTMC-251	Advanced VLSI Design Lab	2	0	0	6	-	-	-	20	30	50
MTMC-25X	Elective Lab	1	0	0	6	-	-	-	20	30	50
Total		**18**	**15**	**0**	**12**						**600**

SCHEME OF EXAMINATION
M. Tech. (Microelectronics)

Second Year: Third Semester Examination

Course Code	Subject Name	Credit	Periods			Evaluation Scheme					Subject Total
						Theory			Practical		
			L	T	P	CT	TA	ESE	TA	ESE	
MTMC-351	Seminar	3	0	0	6	-	-	-	100	-	100
MTMC-352	Dissertation	15	0	0	30	-	-	-	200	300	500
Total		**18**	**0**	**0**	**36**						**600**

Second Year: Fourth Semester Examination

Course Code	Subject Name	Credit	Periods			Evaluation Scheme					Subject Total
						Theory			Practical		
			L	T	P	CT	TA	ESE	TA	ESE	
MTMC-451	Dissertation	18	0	0	36	-	-	-	200	400	600
Total		**18**	**0**	**0**	**36**						**600**

NOTE:

1. The total number of credits of the Program = 64.
2. The grand total of program = 2400
3. Each student shall be required to appear for examination in all courses.
4. Elective course will be offered only if 40% students will opt for a particular course.

Departmental Elective I

MTMC 011: Modeling of Microelectronic Devices
MTMC 012: Designing with ASICS
MTMC 013: Low Power VLSI Design
MTMC 014 Nano-Electronics

Departmental Elective II

MTMC 021: Advance Embedded System
MTMC 022: CMOS RF Design
MTMC 023: VLSI Technology
MTMC 024: FPGA Architecture & Application

Departmental Elective III

MTMC 031: Advanced Microcontroller & System
MTMC 032: Analog Signal Processing
MTMC 033: Analog IC Design
MTMC 034: Microwave Integrated Circuits

Departmental Elective IV

MTMC 041: Hardware Description Languages
MTMC 042: Advanced Computer Architecture
MTMC 043: Digital IC Design
MTMC 044: Advanced Communication Network

Departmental Elective V

MTMC 051: Algorithms for VLSI Design Automation
MTMC 052: MEMS & Micro Sensor Design
MTMC 053: Embedded System for Wireless & Mobile Communication
MT MC054: Artificial Neural Networks

Elective Lab

MTMC 252: Embedded System Lab
MTMC 253: CAD Lab
MTMC 254: Advance Communication Lab

MTMC 101 –Analog CMOS Design

Introduction to Analog VLSI

Analog integrated circuit design, Circuit design consideration for MOS challenges in analog circuit design, recent trends in analog VLSI circuits.

Analog MOSFET Modeling

MOS transistor, Low frequency MOSFET Models, High frequency MOSFET Models, temperature effects in MOSFET, Noise in MOSFET.

Current Source, Sinks and References

MOS Diode/Active resistor, Simple current sinks and mirror, Basic current mirrors, advance current mirror, Current and Voltage references, bandgap references.

CMOS Differential Amplifier

Differential signalling, source coupled pair, Current source load, Common mode rejection ratio, CMOS Differential amplifier with current mirror load,, Differential to single ended conversion.

CMOS Operational amplifier

Block diagram of Op-amplifier, Ideal characteristics of Op-Amplifier, Design of two stage Op-Amplifier, Compensation of Op-Amplifier, Frequency response of Op-Amplifier, Operational Transconductance Amplifier (OTA).

CMOS Comparator

Characteristic of a comparator, Two stage open loop comparator, Special purpose comparator, Regenerative comparator, High output current amplifier, High speed comparator.

Switched Capacitor Circuits

Switched capacitor circuits, Switched capacitor amplifiers, Switch capacitor integrators.

Data converters.

Text/References

1. R. Jacob Baker, H. W. Li, and D.E. Boyce, “CMOS Circuit Design ,Layout and Simulation”, PHI,1998
2. Md. Ismail and Terri Faiz, “Analog VLSI Signal and Information Processing”, McGraw-Hill, 1994
3. Paul R. Gray and R. G. Meyer, “Analysis and design of Analog Integrated circuits”, John Wiley and sons,USA, 3rd Edition, 1993
4. B. Razavi, “RF Microelectronics”, Prentice-Hall PTR,1998
5. David A. Johns and Ken Martin, “Analog Integrated circuit Design, John Wiley & Sons.

MTMC 102 Physical Electronics

Introduction to semiconductor Physics: Review of quantum mechanics, Electrons in periodic lattices, E-k diagrams, Quasiparticles in semiconductors, electrons, holes and phonons. Boltzmann transport equation and solution in the presence of low electric and magnetic fields - mobility and diffusivity; Carrier statistics; Continuity equation, Poisson's equation and their solution; High field effects: velocity saturation, hot carriers and avalanche breakdown.

Semiconductor junctions: Schottky, homo- and hetero-junction band diagrams and I-V characteristics, and small signal switching models; Two terminal and surface states devices based on semiconductor junctions.

MOS structures: Semiconductor surfaces; The ideal and non-ideal MOS capacitor band diagrams and CVs; Effects of oxide charges, defects and interface states; Characterization of MOS capacitors: HF and LF CVs, avalanche injection; High field effects and breakdown.

Characterization of semi conductors: Four probe and Hall measurement; CVs for dopant profile characterization; Capacitance transients and DLTS.

Texts/References

1. J. P. Mc Kelvey, introduction to Solid State and Semiconductor Physics, Harper and Row and John Weathe Hill, 1966.
2. E. H. Nicollian and J. R. Brews, “MOS Physics and Technology,” John Wiley, 1982.
3. K. K. Ng, “Complete Guide to Semiconductor Devices,” McGraw Hill, 1995.
4. D.K. Schroder, “Semiconductor Material and Device Characterization, “John Wiley, 1990.
5. S. M. Sze, “Physics of Semiconductor Devices, “2nd edition John Wiley, 1981.

MTMC 151 – VLSI Circuit Design Lab

Experiments shall be carried out using Tanner/Mentor Graphics/Cadence/Xilinx Tools Session – I:

Digital IC Design Laboratory

1. Introduction to SPICE (Operating Point Analysis, DC Sweep, Transient Analysis, AC Sweep, Parametric Sweep, Transfer Function Analysis)
2. Modeling of Diodes, MOS transistors, Bipolar Transistors etc using SPICE.
3. An Overview of Tanner EDA Tool/MicroWind/Electric/ Magic/LTSpice
4. I-V Curves of NMOS and PMOS Transistors
5. DC Characteristics of CMOS Inverters (VTC, Noise Margin)
6. Dynamic Characteristics of CMOS Inverters (Propagation Delay, Power Dissipation)
7. Schematic Entry/Simulation/ Layout of CMOS Combinational Circuits
8. Schematic Entry/Simulation/ Layout of CMOS Sequential Circuits
9. High Speed and Low Power Design of CMOS Circuits

Session-II: Analog IC Design Laboratory Based

Modeling and Functional Simulation of the following digital circuits (with Xilinx/ ModelSim tools) using VHDL/Verilog Hardware Description Languages

1. Part – I Combinational Logic: Basic Gates,
    a. Multiplexer,
    b. Comparator,
    c. Adder/ Substractor,
    d. Multipliers,
    e. Decoders,
    f. Address Decoders,
    g. Parity generator,
    h. ALU

2. Part – II Sequential Logic:

    a. D-Latch, D-Flip Flop, JK-Flip Flop,
    b. Ripple Counters, Synchronous Counters,
    c. Shift Registers (serial-to-parallel, parallel-to-serial),
    d. Cyclic Encoder / Decoder.

MTMC 152 –Analog Signal Processing Lab

1. Study of MOS Characteristic and Characterization
2. Design and Simulation of Single Stage Amplifiers (Common Source, Source Follower, Common Gate Amplifier)
3. Design and Simulation of Single Stage Amplifiers (Cascode Amplifier, Folded Cascode Amplifier)
4. Design and Simulation of a Differential Amplifier (with Resistive Load, Current Source Biasing)
5. Design and Simulation of Basic Current Mirror, Cascode Current Mirror
6. Analysis of Frequency response of various amplifiers (Common Source, Source Follower, Cascode, Differential Amplifier
7. Design/Simulation/Layout of Telescopic Operational Amplifier/ Folded Cascode Operational Amplifier

Session-II: Analog IC Design Laboratory Based

Modeling and Functional Simulation of the following digital circuits (with Xilinx/ ModelSim tools) using VHDL/Verilog Hardware Description Languages

1. Part – III Memories and State Machines:
    a. Read Only Memory (ROM), Random Access Memory (RAM),
    b. Mealy State Machine, Moore State Machine,
    c. Arithmetic Multipliers using FSMs

2. Part-IV: FPGA System Design:
    a. Demonstration of FPGA and CPLD Boards,
    b. Demonstration of Digital design using FPGAs
    c. CPLDs. Implementation of UART/Mini Processors on FPGA/CPLD etc

MTMC 201 –VLSI Design

UNIT-I The CMOS Inverter: Introduction, The Static CMOS Inverter — An Intuitive Perspective, Evaluating the Robustness of the CMOS Inverter: The Static Behavior, Switching Threshold, Noise Margins, Robustness Revisited, Performance of CMOS Inverter: The Dynamic Behavior, Computing the Capacitances, Propagation Delay: First-Order Analysis, Propagation Delay from a Design Perspective, Power, Energy, and Energy-Delay, Dynamic Power Consumption, Static Consumption, Perspective: Technology Scaling and its Impact on the Inverter Metrics

UNIT-II Designing Combinational Logic Gates in CMOS: Introduction, Static CMOS Design, Complementary CMOS, Ratioed Logic, Pass-Transistor Logic, Dynamic CMOS Design, Dynamic Logic: Basic Principles, Speed and Power Dissipation of Dynamic Logic, Issues in Dynamic Design, Cascading Dynamic Gates, Perspectives, How to Choose a Logic Style, Designing Logic for Reduced Supply Voltages

UNIT-III Designing Sequential Logic Circuits: Introduction, Timing Metrics for Sequential Circuits, Classification of Memory Elements, Static Latches and Registers, The Bistability Principle, Multiplexer -Based Latches Master-Slave Edge-Triggered Register, Low-Voltage Static Latches, Static SR Flip-Flops—Writing Data by Pure Force,

UNIT-IV Dynamic Latches and Registers, Dynamic Transmission-Gate Edge-triggered Registers C2MOS—A Clock-Skew Insensitive Approach, True Single-Phase Clocked Register (TSPCR), Pipelining: An approach to optimize sequential circuits, Latch- vs. Register-Based Pipelines, NORA-CMOS—A Logic Style for Pipelined Structures, Non-Bistable Sequential Circuits, The Schmitt Trigger, Monostable Sequential Circuits, Astable Circuits, Perspective: Choosing a Clocking Strategy.

UNIT-V CMOS Integrated Circuit Layout: Design Rules, Parasitics.Building blocks: ALU's, FIFO's, counters.
Basic Introduction of Physical VLSI system design: data and control path design, floor planning, Physical design methodology

Reference Books:

1. S. M. Kang & Y. Leblebici, “CMOS Digital Integrated Circuits”, McGraw Hill Publication.
2. Jackson & Hodges, “Analysis and Design of Digital Integrated circuits”,. TMH Publication.
3. Ken Martin, “Digital Integrated Circuit Design”, Oxford Publications.
4. Sedra and Smith, “Microelectronic Circuits” Oxford Publications.

MTMC 202 –VLSI Testing and Verification

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends Affecting Testing.

VLSI Testing Process and Test Equipment: How to Test Chips? Automatic Test Equipment, Electrical Parametric Testing. Faults in Digital Circuits: Failures and Faults, Modeling of Faults, Temporary Faults.

Test Generation for Combinational Logic Circuits: Fault Diagnosis of Digital Circuits, Test Generation Techniques for Combinational Circuits, Detection of Multiple Faults in Combinational Logic Circuits. Testable Combinational Logic Circuit Design: The Reed-Mullar Expansion Technique, Three-Level OR-AND-OR Design, Automatic Synthesis of Testing Logic, Testable Design of Multilevel Combinational Circuits, Synthesis of Random Pattern Testable Combinational Circuits, Path Delay Fault Testable Combinational Logic Design, Testable PLA Design.

Test Generation for Sequential Circuits: Testing of Sequential Circuits as Iterative Combinational Circuits, State Table Verification, Test Generation Based on Circuit Structure, Functional Fault Models, Test Generation Based on Functional Fault Models.

Design of Testable Sequential Circuits: Controllability and Observability, Ad Hoc Design Rules for Improving Testability, Design of Diagnosable Sequential Circuits, The Scan-Path Technique for Testable Sequential Circuit Design, Level-Sensitive Scan Design, Random

Access Scan Technique, Partial Scan, Testable Sequential Circuit Design Using Nonscan Techniques, Cross Check, Boundary Scan.

Built-In Self-Test: Test Pattern Generation for BIST, Output Response Analysis, Circular BIST, BIST Architectures.

Testable Memory Design: RAM Fault Models, Test Algorithms for RAMs, Detection of Pattern Sensitive Faults, BIST Techniques for Ram Chips, Test Generation and BIST for Embedded RAMs.

Design verification techniques based on simulation, analytical and formal approaches. Functional verification. Timing verification. Formal verification. Basics of equivalence checking and model checking. Hardware emulation.

Text Books:

1. P. K. Lala, “Digital Circuit Testing and Testability”, Academic Press.
2. M.L. Bushnell and V.D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwar Academic Publishers.
3. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House

   T.Kropf, "Introduction to Formal Hardware Verification", Springer Verlag, 2000.
1. P. Rashinkar, Paterson and L. Singh, "System-on-a-Chip Verification-Methodology and Techniques", Kluwer Academic Publishers, 2001.

MTMC251 – Advanced VLSI Design Lab

Session-I: VLSI System Design

1. Design/Simulation of other Analog building blocks a.
   a. Comparators
   b. Oscillators
   c. PLLs
   d. Switched capacitor circuits
   e. Noise Analysis
2. Mini Projects involving
   a. Unpipelined MIPS Processor
   b. Pipelined MIPS Processor
   c. Out of Order Execution with Tomasulo's Algorithm
   d. Communication Controllers
   e. Arithmetic Circuits
   f. DSP Systems

Session-II: ASIC Design

Experiments shall be carried out using Microwind/System Crafter Tools

1. Part-I: Backend Design

   a. Schematic Entry/ Simulation / Layout/ DRC/PEX/Post Layout Simulation of
   b. CMOS Inverter,
   c. NAND Gate,
   d. OR Gate,
   e. Flip Flops,
   f. Register Cell,
   g. Half Adder,
   h. Full Adder Circuits

2. Part-II: Semicustom Design

   a. HDL Design Entry/ Logic Simulation,
   b. RTL Logic Synthesis,
   c. Post Synthesis Timing Simulation, Place & Route,
   d. Design for Testability, Static Timing Analysis,
   e. Power Analysis of Medium Scale Combinational, Sequential Circuits

3. Part-III: High Speed/Low Power CMOS Design

   a. Designing combinational/sequential CMOS circuits for High Speed Designing

      combinational/sequential CMOS circuits for Low Power

MTMC 011 Modeling of Microelectronic Devices

Unit	Topic	Lectures
1.	**Basic Semiconductor Physics:** Energy bands and Charge Carriers: Solid State Electronic materials, Drift Currents in Semiconductors, Covalent Bond and Energy Bands. Energy Band Model and Fermi Level. MOS Capacitor: Characteristics of the MOS Capacitors, NMOS Transistor, PMOS Transistor, Biasing the MOSFET, Capacitances in MOS Transistor.	**8**
2.	**MOSFET and Compound Semiconductor FET:** Introduction to Scaled MOSFETs, CMOS / BiCMOS, Reliability, SOI and 3D Structures, Memory Structures, Low-Voltage / Low – Power Devices. GaAs MESFETs, Hetero-structure Field-Effect Transistors, Gate Leakage Current, Novel Compound-Semiconductor FETs.	**8**
3.	**Schottky Barriers and Ohmic Contacts:** DC – Current – Voltage Characteristics, Static Model, Large – Signal Model, Small – Signal model.	**8**
4.	**Bipolar Junction Transistors:** Introduction, Principles of Bipolar Transistor Operation, Silicon Bipolar Transistors, Heterojunction Bipolar Transistors, Bipolar Transistor Modelling.	**8**
5.	**Recent Developments in Microelectronic Devices:** Introduction, Transit – Time Diodes, Resonant – Tunnelling Diodes, Transferred – Electron Devices.	**8**

TEXT BOOKS:

1. S M Sze, “Modern Semiconductor Device Physics”, Wiley 1998.
2. R S Muller and T J Kaminis, “Device Electronics for Integrated Circuits”, Second Edition, Wiley 1988.

REFERENCE BOOKS:

1. B G Streetman, “Solid State Electronic Devices”, Fourth Edition PH, 1995.
2. D Foty, “MOSFET Modeling with SPICE: Principles and Practices”, PH, 1997.
3. P W Tulnenga, “SPICE: A Guide to Circuit Simulation and Analysis using PSPICE”, Third Edition, PH, 1995.
4. P Antognetti and C Massobrio, “Semiconductor device and Modeling with SPICE”, Third Edition, PH, 1995.
5. T A Fjeidly, T Ytterdai and M Shun, “Introduction to Device Modeling and Circuit Simulation”, Wiley, 1997.
6. D Nagachoudhari, “Microelectronic Devices”, Pearson 2001.

MTMC 012 –Designing with ASICs

Types of ASICs – Design flow – Economics of ASICs – ASIC cell libraries – CMOS logic cell data path logic cells – I/O cells – cell compilers.

ASIC Library design: Transistors as resistors – parasitic capacitance – logical effort programmable ASIC design software: Design system – logic synthesis – half gate ASIC.

Low level design entry: Schematic entry – low level design languages – PLA tools – EDIF – An overview of VHDL and verilog.

Logic synthesis in verilog and & VHDL simulation.

ASIC Construction – Floor planning & placement – Routing.

Text / References:

J.S. Smith, “Application specific Integrated Circuits”, Addison Wesley, 1997.

MT 013 –Low Power VLSI Design

UNIT I: LOW POWER DESIGN, AN OVER VIEW: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

UNIT II: MOS/BiCMOS PROCESSES: Bi-CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.

UNIT III: LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES: Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/Bi-CMOS processes.

UNIT IV: DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models, Bipolar models. Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

UNIT V: CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS and Bi-CMOS logic gates, Performance Evaluation.

UNIT VI: LOW- VOLTAGE LOW POWER LOGIC CIRCUITS: Comparison of advanced Bi-CMOS Digital circuits. ESD-free Bi-CMOS, Digital circuit operation and comparative Evaluation.

UNIT VII: LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

UNIT VIII: SPECIAL TECHNIQUES: Power Reduction in Clock Networks, CMOS Floating Node, Low Power Bus, Delay Balancing, Low Power Techniques for SRAM.

Text Books:

1. Yeo Rofail/ Gohl, CMOS/BiCMOS ULSI low voltage, low power, PearsonEducation
2. Gary K. Yeap, Practical Low Power Digital VLSI Design, KAP.
3. Douglas A.Pucknell& Kamran Eshraghian, Basic VLSI Design, PHI Publication.
4. J.Rabaey, Digital Integrated circuits, PHI Publication.
5. Sung-mo Kang and Yusuf Leblebici, CMOS Digital ICs, TMH Publication .
   IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.

MTMC 014 Nano Technology 3 1 0

Unit	Topic	Lectures
1.	**Introduction** to nano scale systems, Length energy and time scales, Top down approach to Nano lithography, Spatial resolution of optical, deep ultraviolet, X-ray, electron beam and ion beam lithography, Single electron transistors, coulomb blockade effects in ultra small metallic tunnel junctions.	**8**
2.	**Quantum Mechanics** Quantum confinement of electrons in semiconductor nano structures, Two dimensional confinement (Quantum wells), Band gap engineering, Epitaxy, Landaeur – Buttiker formalism for conduction in confined geometries,	**8**
3.	**One Dimensional Confinement**, Quantum point contacts, quantum dots and Bottom up approach, Introduction to quantum methods for information processing.	**8**
4.	**Molecular Techniques** Molecular Electronics, Chemical self assembly, carbon nano tubes, Self assembled mono layers, Electromechanical techniques,	**8**
5.	**Applications** in biological and chemical detection, Atomic scale characterization techniques, scanning tunnelling microscopy, atomic force microscopy	**8**

TEXT BOOKS:

1. Beenaker and Van Houten "Quantum Transport in Semiconductor Nanostructures in Solid state Physics" Ehernreich and Turnbell, Academic press, 1991.

REFERENCE BOOKS:

1. David Ferry "Transport in Nano structures" Cambridge University press 2000.
2. Y. Imry "Introduction to Mesoscopic Physics, Oxford University press 1997.
3. S. Dutta "Electron Transport in Mesoscopic systems" Cambridge University press 1995.
4. H Grabert and M Devoret "Single charge Tunneling" Plenum press 1992.

MTMC 021 –Advanced Embedded Systems

Typical Embedded System: Core of the Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware,Other System Components.

Characteristics and Quality Attributes of Embedded Systems: Hardware Software Co-Design and Program Modeling: Fundamental Issues inHardware Software Co-Design, Computational Models in Embedded Design, Introduction to Unified Modeling Language, Hardware SoftwareTrade-offs.

Embedded Hardware Design and Development :EDA Tools, How to Use EDA Tool, Schematic Design – Place wire, Bus , port, junction,creating part numbers, Design Rules check, Bill of materials, Netlist creation , PCB Layout Design – Building blocks, Component placement,PCB track routing.

ARM -32 bit Microcontroller family. Architecture of ARM Cortex M3 –General Purpose Registers, Stack Pointer, Link Register, ProgramCounter, Special Register,.Nested Vector Interrupt Controller. Interrupt behavior of ARM Cortex M3. Exceptions Programming. AdvancedProgramming Features.Memory Protection. Debug Architecture.

Embedded Firmware Design and Development: Embedded Firmware Design Approaches, Embedded Firmware Development Languages

Real-Time Operating System (RTOS) based Embedded System Design: Operating System Basics, Types of OS, Tasks, Process and Threads,Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, TaskSynchronization, Device Drivers, How to Choose an RTOS.

The Embedded System Development Environment: The Integrated Development Environment (IDE), Types of Files Generated on Crosscompilation, Disassembler/ELDompiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan.

Text Books:

1. Shibu K V, “Introduction to Embedded Systems”, Tata McGraw Hill Education Private Ltd
2. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M3”, Newnes, (Elsevier).

James K Peckol, “Embedded Systems – A contemporary Design Tool”, John Weily& Sons.

MTMC 022 CMOS RF Design 3 1 0

Unit	Topic		Lectures
1.	**Introduction to RF design** and Wireless Technology: Design and Applications, Complexity and Choice of Technology. Basic concepts in RF design: Nonlinearly and Time Variance, Inter-symbol interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion.		**8**
2.	**RF Modulation**: Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection, Mobile RF communication and basics of Multiple Access techniques. Receiver and Transmitter architectures. Direct conversion and two-step transmitters.		**8**
3.	**RF Testing**: RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.		**8**
4.	**BJT and MOSFET Behavior at RF Frequencies**: BJT and MOSFET behavior at RF frequencies, Modeling of the transistors and SPICE model, Noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation		**8**
5.	**RF Circuits Design:** Overview of RF Filter design, Active RF components & modeling, Matching and Biasing Networks. Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, Various mixers-working and implementation. Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers-PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design, Liberalization techniques, Design issues in integrated RF filters.		**8**

TEXT BOOKS:

1. Ludwig R, Bretchko P, "RF Circuits Design", Pearson 2000 Ed
2. Thomas H. Lee "Design of CMOS RF Integrated Circuits" Cambridge University press 1998.

REFERENCE BOOKS:

1. B Razavi "RF Microelectronics" PHI 1998
2. R Jacob Baker, H W Li, D E Boyce " CMOS Circuit Design, layout and Simulation" PHI 1998
3. Y P Tsividis "Mixed Analog and Digital Devices and Technology" TMH 1996

MTMC 023 VLSI Technology

Environment for VLSI Technology: Clean room and safety requirements. Wafer cleaning processes and wet chemical etching techniques.

Impurity incorporation: Solid State diffusion modeling and technology; Ion Implantation modeling, technology and damage annealing; characterization of Impurity profiles.

Oxidation: Kinetics of Silicon dioxide growth both for thick, thin and ultra thin films. Oxidation technologies in VLSI and ULSI; Characterisation of oxide films; High k and low k dielectrics for ULSI.

Lithography : Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI; Mask generation.

Chemical Vapour Deposition techniques: CVD techniques for deposition of poly silicon, silicon dioxide, silicon nitride and metal films; Epitaxial growth of silicon; modeling and technology.

Metal film deposition: Evaporation and sputtering techniques. Failure mechanisms in metal interconnects; Multi-level metallization schemes.

Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI.

Process integration for NMOS, CMOS and Bipolar circuits; Advanced MOS technologies.

Texts/References

1. C.Y. Chang and S.M.Sze (Ed), “ULSI Technology,” McGraw Hill Companies Inc, 1996.
2. S.K. Ghandhi, “VLSI Fabrication Principles,” John Wiley Inc., New York, 1983.
3. S.M. Sze (Ed), “VLSI Technology, “2nd Edition, McGraw Hill, 1988.

MTMC 024–FPGA Architecture & Applications

UNIT-I

Programmable Logic ROM, PLA, PAL, PLD, PGA–Features, programming and applications using complex programmable logic devices Altera series–Max 5000/7000 series and Altera FLEX logic–10000 series CPLD, AMD's–CPLD (Mach 1 to 5); Cypress FLASH 370 Device Technology, Lattice PLST's Architectures–3000 Series–Speed Performance and in system programmability.

UNIT-II

FPGAs Field Programmable Gate Arrays–Logic blocks, routing architecture, Design flow, Technology Mapping for FPGAs.

UNIT-III

Case Studies Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT &T–ORCA's (Optimized Reconfigurable Cell Array): ACTEL's–ACT-1,2,3 and their speed performance.

UNIT-IV

Finite State Machines (FSM)-I Top-down Design–State Transition Table, state assignments for FPGAs,Problem of initial state assignmentfor one hot encoding. Derivations of state machine charges. Realization of state machine charts with a PAL.

UNIT-V

Finite State Machines (FSM)-IIAlternative realization for state machine chart using microprogramming.Linked state machines,One–Hot statemachine, Petrinetes for statemachines– basic concepts, properties, Extended petrinetes for parallelcontrollers. Finite State Machine–Case Study, Meta Stability,Synchronization.

UNIT-VI

FSM Architectures and Systems Level Design Architectures centered around non-registered PLDs,State machine designs centered around shift registers,One –Hot design method,Use of ASMs in One –Hot design. K Application of One –Hot method, System level design controller, data path and functional partition.

UNIT-VII

Digital front end Digital Design Tools for (FPGAs & ASICs) using Cadence EDA Tool ("FPGA Advantage") – Design Flow Using FPGAs.

UNIT-VIII

Guidelines and Case Studies Parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers.

Reference Books:

1. P.K.Chan& S. Mourad, Digital Design using Field ProgrammableGate Array, Prentice Hall.
2. S.Trimberger, Edr., Field Programmable Gate Array Technology,Kluwer Academic Pub.
3. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley& Sons, Newyork.
4. S.Brown,R.Francis, J.Rose, Z.Vransic, Field Programmable GateArray,Kluwer Pub.
5. Richard FJinder , "Engineering Digital Design,"Academic press

MTMC 031 –Advanced Microcontrollers and Systems

Motivation for advanced microcontrollers – Low Power embedded systems, On-chip peripherals, low-power RF capabilities. Applications of Microcontrollers.

MSP430 – 16-bit Microcontroller family. CPU architecture, Instruction set, Interrupt mechanism, Clock system, Memory subsystem, bus – architecture. The assembly language and „C programming for MSP-430 microcontrollers.On -chip peripherals. WDT, Comparator, Op-Amp, Timer, Basic Timer, Real Time Clock (RTC), ADC, DAC, Digital I/O. Using the low-power features of MSP430. Clock system, low-power modes, Clock request feature, Low-power programming and interrupts.

ARM -32 bit Microcontroller family. Architecture of ARM Cortex M3 – General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Register,. Nested Vector Interrupt Controller. Interrupt behavior of ARM Cortex M3. Exceptions Programming.Advanced Programming Features.Memory Protection. Debug Architecture.

Applications – Wireless Sensor Networking with MSP430 and Low-Power RF circuits; Pulse Width Modulation(PWM) in Power Supplies.

Reference Books:

1. Joseph Yiu, " The Definitive Guide to the ARM Cortex-M3, , Newnes, (Elsevier).
2. John Davies, " MSP430Microcontorller Basics",Newnes (Elsevier Science).
3. MSP430 Teaching CD-ROM, Texas Instruments.

MTMC 032 Analog Signal Processing

Translinear Bipolar and MOS Circuits: General Translinear principles , various translinear circuits: squarer, divider, square rooting, vector magnitude circuit, multipliers, translinear multiplier etc.

MOS Analog Integrated Circuits: Basic building blocks, differential amplifier pair, various current mirrors, active loads, level shifter, differential to single ended converter, complete N-MOS Op-amp.

Low Voltage Signal Processing: Need of low voltage signal processing, C-MOS Op-amp design: input stages, output stages, frequency response, slew rate etc., BI-CMOS op-amp design, input stages, out put stages, introduction to low voltage filter filters.

Current-Mode Signal Processing: Current-mode compared to voltage mode, continuous time signal processing, current conveyors and their applications, current feedback and its applications.

Selected Recent Topics: Realization of MOS resistors in MOS technology, N-MOS OTA, C-MOS OTA, MOSFET-C and other related circuits, C-MOS transconductor circuits.

Text/References

1. C.Toumazou, F.J. Lidgey and D.G.Haigh, 'Analog IC design: The current-mode approach', Exeter, England: Peter Peregrinus, 1990.
2. M. Ismail and T. Fiez, 'Analog VLSI: Signal and Information Processing', Mc Graw Hill, 1994.
3. B. Razavi, 'Design of Analog CMOS Integrated Circuits', Mc Graw Hill, 2000.
4. A.B.Grebene, ' Bipolar and MOS Analog Integrated Circuit Design', Wiley, 1984.
5. A.S.Sedra and K.C.Smith, ' Microelectronic circuits', Oxford University Press.

MTMC 033 –Analog IC Design

UNIT I

Basic MOS Device Physics: General Considerations, MOSFET as a Switch, MOSFET Structure, MOS Symbols, MOS I/V Characteristics, Threshold Voltage, Derivation of I/V Characteristics, Second-Order Effects, MOS Device Models, MOS Device Layout, MOS Device Capacitances, MOS Small-Signal Model, MOS SPICE models, NMOS versus PMOS Devices, Long-Channel versus Short-Channel Devices.

UNIT II

Single-Stage Amplifiers, Basic Concepts , Common-Source Stage, Common-Source Stage with Resistive Load ,CS Stage with Diode-Connected Load, CS Stage with Current-Source Load, CS Stage with Triode Load, CS Stage with Source Degeneration, Source Follower, Common-Gate Stage, Cascode Stage, Folded Cascode, Choice of Device Models.

UNIT III

Differential Amplifiers, Single-Ended and Differential Operation. Basic Differential Pair, Qualitative Analysis, Quantitative Analysis, Common-Mode Response, Differential Pair with MOS Loads, Gilbert Cell, Passive and Active Current Mirrors, Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors, Large-Signal Analysis, Small-Signal Analysis, Common-Mode Properties

UNIT IV

Frequency Response of Amplifiers, General Considerations, Miller Effect, Association of Poles with Nodes, Common-Source Stage, Source Followers, Common-Gate Stage, Cascode Stage, Differential Pair **Feedback** General Considerations, Properties of Feedback Circuits, Types of Amplifiers, Feedback Topologies, Voltage-Voltage Feedback, Current-Voltage Feedback, Voltage-Current Feedback, Current-Current Feedback, Effect of Loading, Two-Port Network Models, Loading in Voltage-Voltage Feedback, Loading in Current-Voltage Feedback, Loading in Voltage-Current Feedback, Loading in Current-Current Feedback, Summary of Loading Effects, Effect of Feedback on Noise

UNIT V

Operational Amplifiers, General Considerations , Performance Parameters, One-Stage Op Amps, Two-Stage Op Amps , Gain Boosting , Comparison , Common-Mode Feedback . Input Range Limitations, Slew Rate, Power Supply Rejection. Stability and Frequency Compensation General Considerations, Multipole Systems, Phase Margin, Frequency Compensation, Compensation of Two-Stage Op Amps, Slewing in Two-Stage Op Amps, Other Compensation Techniques.

Reference Books:

1. B. Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill Publications/
2. P. R. Gray & R. G. Meyer, “Analysis and Design of Analog Integrated Circuits”, John Wiley Publications.
3. R. Gregorian and Temes, “Analog MOS Intgrated Circuits for Signal Processing”, Wiley Publications.
4. Ken Martin, “Analog Integrated Circuit Design”, Wiley Publications.
5. Sedra and Smith, “Microelectronic Circuits”, Oxford Publications.
6. B.Razavi, “Fundamentals of Microelectronics”, Wiley Publications.

MTMC 041 –Hardware Description Languages

UNIT IHARDWARE MODELING WITH THE VERILOG HDL : Hardware Encapsulation –TheVerilog Module, Hardware Modeling Verilog Primitives, Descriptive Styles, StructuralConnections, Behavioral Description In Verilog, Hierarchical Descriptions of Hardware,Structured (Top Down) Design Methodology, Arrays of Instances, Using Verilog for Synthesis,Language Conventions, Representation of Numbers.

UNIT IILOGIC SYSTEM, DATA TYPES AND OPERATORS FOR MODELING IN VERILOGHDL: User-Defined Primitives, User Defined Primitives – Combinational Behavior User-DefinedPrimitives –Sequential Behavior, Initialization of Sequential Primitives. Verilog Variables, LogicValue Set, Data Types, Strings. Constants, Operators, Expressions and Operands, OperatorPrecedence Models Of Propagation Delay; Built-In Constructs for Delay, Signal Transitions,Verilog Models for Gate Propagation Delay (Inertial Delay), Time Scales for Simulation, VerilogModels for Net Delay (Transport Delay), Module Paths and Delays, Path Delays and Simulation,Inertial Delay Effects and Pulse Rejection.

UNIT III- BEHAVIORAL DESCRIPTIONS IN VERILOG HDL: Verilog Behaviors, BehavioralStatements, Procedural Assignment, Procedural Continuous Assignments, Procedural TimingControls and Synchronization, Intra-Assignment, Delay-Blocked Assignments, Non-BlockingAssignment, Intra-Assignment Delay: Non-Blocking Assignment, Simulation of SimultaneousProcedural Assignments, Repeated Intra Assignment Delay, Indeterminate Assignments andAmbiguity, Constructs for Activity Flow Control, Tasks and Functions, Summary of DelayConstructs in Verilog, System Tasks for Timing Checks, Variable Scope Revisited, ModuleContents, Behavioral Models of Finite State Machines.

UNIT IV- SYNTHESIS OF COMBINATIONAL LOGIC: HDL-Based Synthesis, Technology-Independent Design, Benefits of Synthesis, Synthesis Methodology, Vendor Support, Styles forSynthesis of Combinational Logic, Technology Mapping and Shared Resources, Three StateBuffers, Three State Outputs and Don t Cares, Synthesis of Sequential Logic Synthesis ofSequential Udps, Synthesis of Latches, Synthesis of Edge-Triggered Flip Flops, RegisteredCombinational Logic, Shift Registers and Counters, Synthesis of Finite State Machines, Resets,Synthesis of Gated Clocks, Design Partitions and Hierarchical Structures.

UNIT VSYNTHESIS OF LANGUAGE CONSTRUCTS: Synthesis of Nets, Synthesis of RegisterVariables, Restrictions on Synthesis of “X” and “Z”, Synthesis of Expressions and Operators,Synthesis of Assignments, Synthesis of Case and Conditional Statement, Synthesis of Resets,Timings Controls in Synthesis, Synthesis of Multi-Cycle Operations, Synthesis of Loops,Synthesis if Fork Join Blocks, Synthesis of The Disable Statement Synthesis of User-DefinedTasks, Synthesis of User-Defined Functions, Synthesis of Specify Blocks, Synthesis of CompilerDirectives.

UNIT VI- SWITCH-LEVEL MODELS IN VERILOG: MOS Transistor Technology, Switch LevelModels of MOS Transistors, Switch Level Models of Static CMOS Circuits, Alternative Loadsand Pull Gates, CMOS Transmission Gates. Bio-Directional Gates (Switches), Signal Strengths,Ambiguous Signals, Strength Reduction By Primitives, Combination and Resolution of SignalStrengths, Signal Strengths and Wired Logic. Design Examples in Verilog.

UNIT VII- INTRODUCTION TO VHDL: An Overview of Design Procedures used for System Designusing CAD Tools. Design Entry. Synthesis, Simulation, Optimization, Place and Route. DesignVerification Tools. Examples using Commercial PC Based on VHDL Elements of VHDL TopDown Design with VHDL Subprograms. Controller Description VHDL Operators.

UNIT VIII- BEHAVIORAL DESCRIPTION OF HARDWARE IN VHDL: Process Statement AssertionStatements, Sequential Wait Statements Formatted ASCII I/O Operators, MSI-Based Design.Differences between VHDL and Verilog.

Reference Books:

1. M.D.CILETTI, Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice-Hall.
2. Z.NAWABI, VHDL Analysis and Modeling of Digital Systems, McGraw Hill.
3. M.G.ARNOLD, Verilog Digital – Computer Design”, Prentice-Hall (PTR).
4. PERRY, “VHDL”, McGraw Hill.

MTMC 042 Advanced Computer Architecture

Parallel computer models: The state of computing, Classification of parallel computers, Multiprocessors and multi computers, Multi vector and SIMD computers.

Program and network properties: Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms

System Interconnect Architectures: Network properties and routing, Static interconnection Networks, Dynamic interconnection Networks, Multiprocessor system Interconnects, Hierarchical bus systems, Crossbar switch and multiport memory, Multistage and combining network.

Advanced processors: Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Vector and Symbolic processors

Pipelining: Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multifunctional arithmetic pipelines

Memory Hierarchy Design: Cache basics & cache performance, reducing miss rate and miss penalty, multilevel cache hierarchies, main memory organizations, design of memory hierarchies.

Multiprocessor architectures: Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, MOESI), scalable cache coherence, overview of directory based approaches, design challenges of directory protocols, memory based directory protocols, cache based directory protocols, protocol design tradeoffs, synchronization,

Texts

1. Kai Hwang, “Advanced Computer architecture”; TMH.
2. Advance Microprocessor Senthile Oxford

References

3. D. A. Patterson and J. L. Hennessey, “Computer organization and design,” Morgan Kaufmann, 2nd Ed.
4. J.P.Hayes, “computer Architecture and organization”; MGH.
5. Harvey G.Cragon,”Memory System and Pipelined processors”; Narosa Publication.
6. V.Rajaranam & C.S.R.Murthy, “Parallel computer”; PHI.
7. R.K.Ghose, Rajan Moona & Phalguni Gupta, “Foundation of Parallel Processing”; Narosa Publications.
8. Kai Hwang and Zu, “Scalable Parallel Computers Architecture”; MGH.

MTMC 043 –Digital IC Design

UNIT-I I:ntroduction: Historical Perspective, Issues in Digital Integrated Circuit Design,Quality Metrics of a Digital Design - Cost of an Integrated Circuit, Functionality and Robustness, Performance, Power and Energy Consumption – The Manufacturing Process: Introduction, The Diode, A First Glance at the Diode — The Depletion Region, Static Behavior, Dynamic, or Transient, Behavior, The Actual Diode—SecondaryEffects, The SPICE Diode Model, The MOS(FET) Transistor, A First Glance at the Device, The MOS Transistor under Static Conditions, Dynamic Behavior, The Actual MOS Transistor—Some Secondary Effects, SPICE Models for the MOS Transistor – Wire: Introduction, A First Glance, Interconnect Parameters — Capacitance, Resistance, and Inductance, Capacitance, Resistance, Inductance

UNIT-II : Devices: Binary State Terminology and Mixed Logic Notation, Logic Level Conversion: The Inverter, AND and OR Operators and Their Mixed-Logic Circuit Symbology, Logic Level Incompatibility: Complementation ,Reading and Construction of Mixed-Logic Circuits, Multiple Output Optimization, Entered Variable K-map Minimization, XOR-Type Patterns and Extraction of Gate-Minimum Cover fromEV K-maps, K-map Plotting and Entered Variable XOR Patterns , The SOP-to-EXSOP Reed-Muller Transformation , The POS-to-EQPOS Reed-Muller Transformation ,Examples of Minimum Function Extraction ,Heuristics for CRMT Minimization.

UNIT-III : The CMOS Inverter: Introduction, The Static CMOS Inverter — An Intuitive Perspective, Evaluating the Robustness of the CMOS Inverter: The Static Behavior, Switching Threshold, Noise Margins, Robustness Revisited, Performance of CMOS Inverter: The Dynamic Behavior, Computing the Capacitances, Propagation Delay: First-Order Analysis, Propagation Delay from a Design Perspective, Power, Energy, and Energy-Delay, Dynamic Power Consumption, Static Consumption, Perspective: Technology Scaling and its Impact on the Inverter Metrics

UNIT-IV : Designing Combinational Logic Gates in CMOS: Introduction, Static CMOS Design, Complementary CMOS, Ratioed Logic, Pass-Transistor Logic, Dynamic CMOS Design, Dynamic Logic: Basic Principles, Speed and Power Dissipation of Dynamic Logic, Issues in Dynamic Design, Cascading Dynamic Gates, Perspectives, How to Choose a Logic Style, Designing Logic for Reduced Supply Voltages

UNIT-V : Designing Sequential Logic Circuits: Introduction, Timing Metrics for Sequential Circuits, Classification of Memory Elements, Static Latches and Registers,—, Pipelining: An approach to optimize sequential circuits, Latch- vs. Register-Based Pipelines, NORA-CMOS.A Logic Style for Pipelined Structures, Non-Bistable Sequential Circuits, The Schmitt Trigger, Monostable Sequential Circuits, Astable Circuits, Perspective: Choosing a Clocking Strategy.

Reference Books:

1. Jan M. Rabaey Anantha Chandrakasan, &Borivoje Nikolic, “Digital Integrated Circuits – A design perspective”, PHI Publication.
2. S. M. Kang & Y. Leblebici, “CMOS Digital Integrated Circuits”, McGraw Hill Publication.
3. Richard F Tinder“Engineering Digital Design”,Academic Press
4.Jackson & Hodges, “Analysis and Design of Digital Integrated circuits”,. TMH Publication.
5. Ken Martin, “Digital Integrated Circuit Design”, Oxford Publications.

MTMC 044 Advanced Communications Network

Overview of Internet-Concepts, challenges and history. Overview of high speed networks-ATM. TCP/IP Congestion and Flow Control in Internet-Throughput analysis of TCP congestion control. TCP for high bandwidth delay networks. Fairness issues in TCP.

Real Time Communications over Internet. Adaptive applications. Latency and throughput issues. Integrated Services Model (intServ). Resource reservation in Internet. RSVP.

Characterization of Traffic by Linearly Bounded arrival Processes (LBAP). Concept of (o,, p) regulator. Leaky bucket algorithm and its properties.

Packet Scheduling Algorithms-requirements and choices. Scheduling guaranteed service connections. GPS, WFQ and Rate proportional algorithms. High speed scheduler design. Theory of Latency Rate servers and delay bounds in packet switched networks for LBAP traffic.

Active Queue Management - RED, WRED and Virtual clock. Control theoretic analysis of active queue management.

IP address lookup-challenges. Packet classification algorithms and Flow Identification- Grid of Tries, Cross producting and controlled prefix expansion algorithms.

Admission control in Internet. Concept of Effective bandwidth. Measurement based admission control. Differentiated Services in Internet (DiffServ). DiffServ architecture and framework.

IP switching and MPLS-Overview of IP over ATM and its evolution to IP switching. MPLS architecture and framework. MPLS Protocols. Traffic engineering issues in MPLS. [P control of Optical Routers. Lamda Switching, DWDM Networks

Text/References

1. Jean Wairand and Pravin Varaiya, High Perforamnce Communications Networks, Second Edition, 2000.
2. Jean Le Boudec and Patrick Thiran, Network Calculus A Theory of Deterministic Queueing Systems for the Internet, Springer Veriag, 2001.
3. Zhang Wang, Internet Qo,5, Morgan Kaufman 2001.

MTMC 051 –Algorithms for VLSI Design Automation

VLSI physical design automation and Fabrication VLSI Design cycle, New trends in VLSI design, Physical design cycle, Design style, Introduction to fabrication process, design rules, layout of basic devices

VLSI automation Algorithms Partitioning: Problem formulation, classification ofpartitioning algorithms, Group migration algorithms, simulated annealing.

Floor planning & pin assignment: Problem formulation, classification of floorplanning algorithms, constraint based floor planning, floor planning algorithms for mixedblock& cell design, chip planning, pin assignment, problem formulation, classificationof pin assignment algorithms, General & channel pin assignment Placement Problemformulation, classification of placement algorithms, simulation base placementalgorithms, recent trends in placement

Global Routing and Detailed routing: Problem formulation, classification of global routingalgorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms,performance driven routing Detailed routing problem formulation, classification ofrouting algorithms, introduction to single layer routing algorithms, two layer channelrouting algorithms, greedy channel routing, switchbox routing algorithms.

Over the cell routing & via minimization: Two layers over the cell routers,constrained& unconstrained via minimization

Compaction: Problem formulation, classification of compaction algorithms, onedimensionalcompaction, two dimension based compaction, hierarchical compaction

Reference Books :

1. NaveedShervani, "Algorithms for VLSI physical design Automation", KluwerAcademic Publisher, Second edition.
2. ChristophnMeinel& Thorsten Theobold, "Algorithm and Data Structures for VLSIDesign", Kluwer Academic Publisher.
3. R. Drechsler, "Evolutionary Algorithm for VLSI CAD", Kluwer Academic Publication.

MTMC 052 –MEMS & Micro Sensor Design

Introduction to MEMS

MEMS Fabrication Technologies, Materials and Substrates for MEMS, Processes forMicromachining, Characteristics, Sensors/Transducers, Piezoresistance Effect,Piezoelectricity, Piezoresistive Sensor.

Mechanics of Beam and Diaphragm Structures

Stress and Strain, Hooke's Law. Stress and Strain of Beam Structures: Stress, Strain in aBent Beam, Bending Moment and the Moment of Inertia, Displacement of BeamStructures Under Weight, Bending of Cantilever Beam Under Weight.

Air Damping

Drag Effect of a Fluid: Viscosity of a Fluid, Viscous Flow of a Fluid, Drag ForceDamping, The Effects of Air Damping on Micro-Dynamics. Squeeze-film Air Damping:Reynolds' Equations for Squeeze-film Air Damping, Damping of Perforated ThickPlates. Slide-film Air Damping: Basic Equations for Slide-film Air Damping,Couette-flow Model, Stokes-flow Model.

Electrostatic Actuation Electrostatic Forces, Normal Force, Tangential Force, Fringe Effects, ElectrostaticDriving of Mechanical Actuators: Parallel -plate Actuator, Capacitive sensors. Step and Alternative Voltage Driving: Step Voltage Driving, Negative SpringEffect and Vibration Frequency.

Thermal Effects

Temperature coefficient of resistance, Thermo-electricity, Thermocouples, Thermal andtemperature sensors.

Applications of MEMS in RF

MEMS Resonator Design Considerations, One-Port Micromechanical ResonatorModeling Vertical Displacement Two-Port Microresonator Modeling,Micromechanical Resonator Limitations.

Reference Books:

1. S.M. Sze, “Semiconductor Sensors”, John Wiley & Sons Inc., Wiley Interscience Pub.
2. M.J. Usher, “Sensors and Transducers”, McMillian Hampshire.
3. RS Muller, Howe, Senturia and Smith, “Micro sensors”, IEEE Press.

MTMC 053 –Embedded System for Wireless & Mobile Communication

Typical Embedded System: Core of the Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware, Other System Components.

Characteristics and Quality Attributes of Embedded Systems: Hardware Software Co-Design and Program Modeling: Fundamental Issues in Hardware Software Co-Design, Computational Models in Embedded Design, Introduction to Unified Modeling Language, Hardware Software Trade-offs.

Introduction to wireless technologies: WAP services, Serial and Parallel Communication, Asynchronous and synchronous Communication, FDM,TDM, TFM, Spread spectrum technology.

Introduction to Bluetooth: Specification, Core protocols, Cable replacement protocol
Bluetooth Radio: Type of Antenna, Antenna Parameters, Frequency hoping

Bluetooth Networking: Wireless networking, wireless network types, devices roles and states, adhoc network, scatter net Connection establishment procedure, notable aspects of connection establishment, Mode of connection, Bluetooth security, Security architecture, Security level of services, Profile and usage model: Generic access profile (GAP), SDA, Serial port profile,

Secondary Bluetooth profile Hardware: Bluetooth Implementation, Baseband overview, packet format, Transmission buffers, Protocol Implementation: Link Manager Protocol, Logical Link Control Adaptation Protocol, Host control Interface, Protocol Interaction with layers

Programming with Java: Java Programming, J2ME architecture, Javax. Bluetooth package Interface, classes, exceptions, Javax. obex Package: interfaces, classes

Bluetooth services registration and search application, Bluetooth client and server application.
Overview of IrDA, Home RF, Wireless LANs, JINI

Reference Books:

1. hibu K V, “Introduction to Embedded Systems”, Tata McGraw Hill Education Private Ltd

1. C.S.R. Prabhu and A.P. Reddi,“ Bluetooth Technology”, PHI Publication.
2. U. Dalal& M. Shukla, "Wireless & Mobile Communication", Oxford University Press.
3. C. Y. William, Lee, "Mobile communication engineering theory and applications", TMH, Publication.
4. S .Haykins, “Communication Systems”, John Wiley and Sons.

MTMC 054 Artificial Neural Networks

Introduction: Biological neurons and memory: Structure and function of a single neuron; Artificial Neural Networks (ANN); Typical applications of ANNs : Classification, Clustering, Vector Quantization, Pattern Recognition, Function Approximation, Forecasting, Control, Optimization; Basic Approach of the working of ANN - Training, Learning and Generalization.

Supervised Learning: Single-layer networks; Perceptron-Linear separability, Training algorithm, Limitations; Multi-layer networks-Architecture, Back Propagation Algorithm (BTA) and other training algorithms, Applications. Adaptive Multi-layer networks-Architecture, training algorithms; Recurrent Networks; Feed-forward networks; Radial-Basis-Function (RBF)
networks.

Unsupervised Learning: Winner-takes-all networks; Hamming networks; Maxnet; Simple competitive learning; Vector-Quantization; Counter propagation networks; Adaptive Resonance Theory; Kohonen's Self-organizing Maps; Principal Component Analysis.

Associated Models: Hopfield Networks, Brain-in-a-Box network; Boltzmann machine.

Optimization Methods: Hopfield Networks for-TSP, Solution of simultaneous linear equations; Iterated Gradient Descent; Simulated Annealing; Genetic Algorithm.

Texts/References

1. K. Mehrotra, C.K. Mohan and Sanjay Ranka, Elements of Artificial Neural Networks, MIT Press, 1997 - [Indian Reprint Penram International Publishing (India), 1997]
2. Simon Haykin, Neural Networks - A Comprehensive Foundation, Macmillan Publishing Co., New York, 1994.
3. A Cichocki and R. Unbehauen, Neural Networks for Optimization and Signal Processing, John Wiley and Sons, 1993.
4. J. M. Zurada, Introduction to Artificial Neural Networks, (Indian edition) Jaico Publishers, Mumbai, 1997.