Course Structure & Scheme

For

Master of Technology

In

Microelectronics

Electronics Engineering Department
Institute of Engineering and Technology
AKTU Technical University, Lucknow - 226 021
www.ietlucknow.edu*, *www.aktu.ac.in

Eligibility Condition

1. B. Tech / B.E in Electronics & Communication / Electronics and Instrumentation/ Electrical and Electronics Engineering/ or equivalent degree with 60% marks.

Admission Procedure

Post Graduate admissions norms decided by AKTU

Admission Intake per batch

Total of 15 students per batch

SCHEME OF EXAMINATION
M. Tech. (Microelectronics)

First Year:First Semester

Course Code	Subject Name	Credit	Periods			Evaluation Scheme					Subject Total
						Theory			Practical		
			L	T	P	CT	TA	ESE	TA	ESE	
MTMC-101	Analog CMOS Circuit	3	3	1	0	20	10	70	-	-	100
MTMC-102	Physical Electronic	3	3	1	0	20	10	70	-	-	100
MTMC-01X	Elective - I	3	3	1	0	20	10	70	-	-	100
MTMC-02X	Elective - II	3	3	1	0	20	10	70	-	-	100
	Research Process & Methodology	3	3	1	0	20	10	70	-	-	100
MTMC-151	VLSI Circuit Design Lab	2	0	0	6	-	-	-	20	30	50
MTMC-152	Analog Signal Processing Lab	1	0	0	6	-	-	-	20	30	50
Total		**18**	**15**	**0**	**12**						**600**

SCHEME OF EXAMINATION
M. Tech. (Microelectronics)

First Year: Second Semester

Course Code	Subject Name	Credit	Periods			Evaluation Scheme					Subject Total
						Theory			Practical		
			L	T	P	CT	TA	ESE	TA	ESE	
MTMC-201	VLSI Design	3	3	1	0	20	10	70	-	-	100
MTMC-202	VLSI Testing & Verification	3	3	1	0	20	10	50	-	-	100
MTMC-03X	Elective - III	3	3	1	0	20	10	50	-	-	100
MTMC-04X	Elective - IV	3	3	1	0	20	10	50	-	-	100
MTMC-05X	Elective - V	3	3	1	0	20	10	50	-	-	100
MTMC-251	Advanced VLSI Design Lab	2	0	0	6	-	-	-	20	30	50
MTMC-25X	Elective Lab	1	0	0	6	-	-	-	20	30	50
Total		**18**	**15**	**0**	**12**						**600**

SCHEME OF EXAMINATION
M. Tech. (Microelectronics)

Second Year: Third Semester

Course Code	Subject Name	Credit	Periods			Evaluation Scheme					Subject Total
						Theory			Practical		
			L	T	P	CT	TA	ESE	TA	ESE	
MTMC-351	Seminar	3	0	0	6	-	-	-	100	-	100
MTMC-352	Dissertation	15	0	0	30	-	-	-	200	300	500
Total		**18**	**0**	**0**	**36**						**600**

Second Year: Fourth Semester

Course Code	Subject Name	Credit	Periods			Evaluation Scheme					Subject Total
						Theory			Practical		
			L	T	P	CT	TA	ESE	TA	ESE	
MTMC-451	Dissertation	18	0	0	36	-	-	-	200	400	600
Total		**18**	**0**	**0**	**36**						**600**

NOTE:

1. The total number of credits of the Program = 64.
2. The grand total of program = 2400
3. Each student shall be required to appear for examination in all courses.
4. Elective course will be offered only if 40% students will opt for a particular course.

List of Electives offered by the Department:

Departmental Elective I

MTMC 011: Modeling of Microelectronic Devices
MTMC 012: Designing with ASICS
MTMC 013: Low Power VLSI Design
MTMC 014 Nano-Electronics

Departmental Elective II

MTMC 021: Advance Embedded System
MTMC 022: CMOS RF Design
MTMC 023: VLSI Technology
MTMC 024: FPGA Architecture & Application

Departmental Elective III

MTMC 031: Advanced Microcontroller & System
MTMC 032: Analog Signal Processing
MTMC 033: Analog IC Design
MTMC 034: Microwave Integrated Circuits

Departmental Elective IV

MTMC 041: Hardware Description Languages
MTMC 042: Advanced Computer Architecture
MTMC 043: Digital IC Design
MTMC 044: Advanced Communication Network

Departmental Elective V

MTMC 051: Algorithms for VLSI Design Automation
MTMC 052: MEMS & Micro Sensor Design
MTMC 053: Embedded System for Wireless & Mobile Communication
MT MC054: Artificial Neural Networks

Elective Lab

MTMC 252: Embedded System Lab
MTMC 253: CAD Lab
MTMC 254: Advance Communication Lab

MTMC-101	ANALOG CMOS DESIGN	L: 3	T: 1	P: 0	Credits : 3

Course Objective: Students undergoing this course are expected to:

1. Understand the basics of MOS device physics and its operation.
2. Understand the various operations of current mirror and differential amplifier using CMOS.
3. Attain knowledge about characteristics of Two stage operational amplifier and Operational Transconductance Amplifier using CMOS.
4. To understand the principles of comparators
5. Understand the concept of Switched capacitor technique and data converter in CMOS technologies.

Syllabus:

Unit	Topics	Lectures
I	Introduction to Analog VLSI, Analog integrated circuit design, Circuit design consideration for MOS challenges in analog circuit design, recent trends in analog VLSI circuits, Analog MOSFET Modeling (MOS transistor, Low frequency MOSFET Models, High frequency MOSFET Models, temperature effects in MOSFET, Noise in MOSFET)	8
II	Current Source, Sinks and References, MOS Diode/Active resistor, Simple current sinks and mirror, Basic current mirrors, advance current mirror, Current and Voltage references, bandgap references	8
III	CMOS Differential Amplifier, Differential signaling, source coupled pair, Current source load, Common mode rejection ratio, CMOS Differential amplifier with current mirror load, Differential to single ended conversion	8
IV	CMOS Operational amplifier, Block diagram of Op-amplifier, Ideal characteristics of Op-Amplifier, Design of two stage Op-Amplifier, Compensation of Op-Amplifier, Frequency response of Op-Amplifier, Operational Transconductance Amplifier (OTA)	8
V	CMOS Comparator, Characteristic of a comparator, Two stage open loop comparator, Special purpose comparator, Regenerative comparator, High output current amplifier, High speed comparator, Switched Capacitor Circuits, Switched capacitor circuits, Switched capacitor amplifiers, Switch capacitor integrators, Data converters	8

Text/References

1. R. Jacob Baker, H. W. Li, and D.E. Boyce, "CMOS Circuit Design ,Layout and Simulation", PHI,1998
2. Md. Ismail and Terri Faiz, "Analog VLSI Signal and Information Processing", McGraw-Hill, 1994
3. Paul R. Gray and R. G. Meyer, "Analysis and design of Analog Integrated circuits", John Wiley and sons,USA, 3rd Edition, 1993
4. B. Razavi, "RF Microelectronics", Prentice-Hall PTR,1998
5. David A. Johns and Ken Martin, "Analog Integrated circuit Design, John Wiley & Sons.

Course Outcomes:

CO101.1	Recall the basic basics of MOSFET device physics and its operation
CO101.2	Understanding the operations of current mirror and differential amplifier using CMOS
CO101.3	Design the circuit of operational amplifier, Two stage operational amplifier and Operational Transconductance Amplifier using CMOS
CO101.4	Design the principles of comparators
CO101.5	Understand concept of Switched capacitor technique and data converter in CMOS technologies

MTMC-102	Physical Electronics	L: 3	T: 1	P: 0	Credits : 3

Course Objective: After completion of this course student will be able to:

1. Understand the semiconductor physics and quantum mechanics
2. Knowledge about Energy band diagram and current in semiconductor material
3. Knowledge about the different types of diode and their characteristics
4. Understand the working of MOS capacitor, MOSFET, BJT and their characteristics

Syllabus:

Unit	Topics	Lectures
I	Introduction to Semiconductor Physics- Review of quantum mechanics, Electrons in periodic lattices, E-k diagrams, Quasiparticles in semiconductors, electrons, holes and phonons	8
II	Boltzmann transport equation and solution- Mobility and diffusivity, Carrier statistics, Continuity equation, Poisson's equation and their solution, High field effects: velocity saturation, hot carriers and avalanche breakdown	8
III	Semiconductor junctions- Schottky, homo- and hetero-junction band diagrams and I-V characteristics, and small signal switching models; Two terminal and surface states devices based on semiconductor junctions	8
IV	MOS structures- Semiconductor surfaces; The ideal and non-ideal MOS capacitor band diagrams and CVs; Effects of oxide charges, defects and interface states; Characterization of MOS capacitors: HF and LF CVs, avalanche injection; High field effects and breakdown	8
V	Characterization of Semiconductors- Four probe and Hall measurement; CVs for dopant profile characterization; Capacitance transients and DLTS	8

Texts/References

1. J. P. Mc Kelvey, introduction to Solid State and Semiconductor Physics, Harper and Row and John Weathe Hill, 1966.
2. E. H. Nicollian and J. R. Brews, “MOS Physics and Technology,” John Wiley, 1982.
3. K. K. Ng, “Complete Guide to Semiconductor Devices,” McGraw Hill, 1995.
4. D.K. Schroder, “Semiconductor Material and Device Characterization, “John Wiley, 1990.
5. S. M. Sze, “Physics of Semiconductor Devices, “2nd edition John Wiley, 1981.

Course Outcomes:

CO102.1	To develop the understanding of intrinsic and extrinsic semiconductor material and crystal lattice structure
CO102.2	Understanding of energy band diagram at 0K and 300K of semiconductor material and current phenomenon in semiconductor material
CO102.3	Understanding of depletion layer of P-N junction diode and I-V characteristics
CO102.4	To develop the understanding of energy band diagram of different types of diode
CO102.5	To develop the understanding of accumulation depletion and inversion mode in MOS capacitor, I-V characteristics of MOSFET

MTMC-151	VLSI Circuit Design Lab	L: 0	T: 0	P: 6	Credits : 2

Course Objective: Students undergoing this course are expected to:

1. Familiar with Xilinx to perform the circuit analysis.
2. To perform the analysis and layout designing of the circuit.
3. Calculate all the performance parameters of the implemented circuits.
4. Perform programming on Sparton kit.

Experiments shall be carried out using Tanner/Mentor Graphics/Cadence/Xilinx Tools Session – I:

Digital IC Design Laboratory

1. Introduction to SPICE (Operating Point Analysis, DC Sweep, Transient Analysis, AC Sweep, Parametric Sweep, Transfer Function Analysis)
2. Modeling of Diodes, MOS transistors, Bipolar Transistors etc using SPICE.
3. An Overview of Tanner EDA Tool/MicroWind/Electric/ Magic/LTSpice
4. I-V Curves of NMOS and PMOS Transistors
5. DC Characteristics of CMOS Inverters (VTC, Noise Margin)
6. Dynamic Characteristics of CMOS Inverters (Propagation Delay, Power Dissipation)
7. Schematic Entry/Simulation/ Layout of CMOS Combinational Circuits
8. Schematic Entry/Simulation/ Layout of CMOS Sequential Circuits
9. High Speed and Low Power Design of CMOS Circuits

Session-II: Analog IC Design Laboratory Based

Modeling and Functional Simulation of the following digital circuits (with Xilinx/ ModelSim tools) using VHDL/Verilog Hardware Description Languages

1. Part – I Combinational Logic: Basic Gates,
    a. Multiplexer,
    b. Comparator,
    c. Adder/ Substractor,
    d. Multipliers,
    e. Decoders,
    f. Address Decoders,
    g. Parity generator,
    h. ALU
2. Part – II Sequential Logic:
    a. D-Latch, D-Flip Flop, JK-Flip Flop,
    b. Ripple Counters, Synchronous Counters,
    c. Shift Registers (serial-to-parallel, parallel-to-serial),
    d. Cyclic Encoder / Decoder.

Course Outcomes:

CO151.1	Familiar with HDLs to perform the circuit simulation.
CO151.2	To perform the analysis and layout designing of the circuit.
CO151.3	Calculate all the performance parameters of the implemented circuits.
CO151.4	Obtain results from Sparton Kit.

MTMC-152	Analog Signal Processing Lab	L: 0	T: 0	P: 6	Credits : 1

Course Objective: student will be able to:

1. Attain knowledge about the functionality and components of the Analog System Lab Kit PRO.
2. Discover the fundamental concepts of operational amplifiers (op-amps) and their applications in analog signal processing.
3. Analyze the principles and working of multivibrator circuits using operational amplifiers (op-amps).
4. Apply theoretical concepts to analyze the stability and response time of Automatic Gain Controlled circuits under varying input conditions.
5. Gain the knowledge of op-amp based circuits to meet specific application requirements.

List of Experiments

1. Study of MOS Characteristic and Characterization
2. Design and Simulation of Single Stage Amplifiers (Common Source, Source Follower, Common Gate Amplifier)
3. Design and Simulation of Single Stage Amplifiers (Cascode Amplifier, Folded Cascode Amplifier)
4. Design and Simulation of a Differential Amplifier (with Resistive Load, Current Source Biasing)
5. Design and Simulation of Basic Current Mirror, Cascode Current Mirror
6. Analysis of Frequency response of various amplifiers (Common Source, Source Follower, Cascode, Differential Amplifier
7. Design/Simulation/Layout of Telescopic Operational Amplifier/ Folded Cascode Operational Amplifier

Session-II: Analog IC Design Laboratory Based

Modeling and Functional Simulation of the following digital circuits (with Xilinx/ ModelSim tools) using VHDL/Verilog Hardware Description Languages

1. Part – III Memories and State Machines:
    a. Read Only Memory (ROM), Random Access Memory (RAM),
    b. Mealy State Machine, Moore State Machine,
    c. Arithmetic Multipliers using FSMs
2. Part-IV: FPGA System Design:
    a. Demonstration of FPGA and CPLD Boards,
    b. Demonstration of Digital design using FPGAs
    c. CPLDs. Implementation of UART/Mini Processors on FPGA/CPLD etc

Course Outcomes:

CO1	Attain knowledge about the functionality and components of the Analog System Lab Kit PRO.
CO2	Discover the fundamental concepts of operational amplifiers (op-amps) and their applications in analog signal processing.
CO3	Analyze the principles and working of multivibrator circuits using operational amplifiers.
CO4	Apply theoretical concepts to analyze the stability and response time of Automatic Gain Controlled circuits under varying input conditions.
CO5	Gain the knowledge of op-amp based circuits to meet specific application requirements.

MTMC-201	VLSI Design	L: 3	T: 1	P: 0	Credits : 3

Course Objective: Students undergoing this course are expected to:

1. To understand the various principles and techniques of designing combinational logic gates in CMOS technology.
2. To teach various principles and techniques of designing combinational logic gates in CMOS technology.
3. To study design and optimize sequential logic circuits.
4. To study digital circuits using various logic methods and their limitations.
5. To highlight the circuit design issues in the context of VLSI technology.

Syllabus:

Unit	Topics	Lectures
I	The CMOS Inverter: Introduction, The Static CMOS Inverter An Intuitive Perspective, Evaluating the Robustness of the CMOS Inverter: The Static Behavior, Switching Threshold, Noise Margins, Robustness Revisited, Performance of CMOS Inverter: The Dynamic Behavior, Computing the Capacitances, Propagation Delay: First Order Analysis, Propagation Delay from a Design Perspective, Power, Energy, and Energy Delay, Dynamic Power Consumption, Static Consumption, Perspective: Technology Scaling and its Impact on the Inverter Metrics	10
II	Designing Combinational Logic Gates in CMOS: Introduction, Static CMOS Design, Complementary CMOS, Ratioed Logic, Pass Transisto r Logic, Dynamic CMOS Design, Dynamic Logic: Basic Principles, Speed and Power Dissipation of Dynamic Logic, Issues in Dynamic Design, Cascading Dynamic Gates, Perspectives, How to Choose a Logic Style, Designing Logic for Reduced Supply Voltages	12
III	Introduction, Timing Metrics for Sequential Circuits, Classification of Memory Elements, Static Latches and Registers, The Bistability Principle, Multiplexer Based Latches Master Slave Edge Triggered Register, Low Voltage Static Latches, Static SR Flip Flops Writing Data by Pure Force.	7
IV	Dynamic Latches and Registers, Dynamic Transmission Gate Edge triggered Registers C2MOS A Clock Skew Insensitive Approach, True Single Phase Clocked Register (TSPCR), Pipelining: An approach to optimize sequential circuits, Latch vs. Register Based Pipelines, NORA CMOS A Logic Style for Pipelined Structures, Non Bistable Sequential Circuits, The Schmitt Trigger, Monostable Sequential Circuits, Astable Circuits,Perspec tive: Choosing a Clocking Strategy	7
V	CMOS Integrated Circuit Layout: Design Rules, Parasitics.Building blocks: ALU's, FIFO's, counters. Basic Introduction of Physical VLSI system design: data and control path design, floor planning, Physical design methodology	6

Reference Books:

1. S. M. Kang & Y. Leblebici, “CMOS Digital Integrated Circuits”, McGraw Hill Publication.
2. Jackson & Hodges, “Analysis and Design of Digital Integrated circuits”,. TMH Publication.
3. Ken Martin, “Digital Integrated Circuit Design”, Oxford Publications.
4. Sedra and Smith, “Microelectronic Circuits” Oxford Publications.

Course Outcomes:

CO201.1	Recall the basic fundamental principles of CMOS inverter circuit with its design techniques to optimize their operation.
CO201.2	Understand the various principles and techniques of designing combinational logic gates in CMOS technology.
CO201.3	Design and optimize sequential logic circuits.
CO201.4	Understand digital circuits using various logic methods and their limitations.
CO201.5	Understand the design model, method, criterion and steps of physical design methodology.

MTMC-202	VLSI TESTING AND VERIFICATION	L: 3	T: 1	P: 0	Credits : 3

Course Objective: Students undergoing this course are expected to:

1. Analyze the use of procedural statements and routines in testbench design with system verilog.
2. Apply fault modeling concepts in designing testbench.
3. IDDQ fault modeling and testing application specific memory testing
4. To learn RAM fault modeling and testing for memory
5. Understand use of functional and formal verification in test design.

SYLLABUS:

Unit	Topics	Lectures
I	Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends Affecting Testing.VLSI Testing Process and Test Equipment: How to Test Chips? Automatic Test Equipment, Electrical Parametric Testing. Faults in Digital Circuits: Failures and Faults, Modeling of Faults, Temporary Faults.	10
II	Test Generation for Combinational Logic Circuits: Fault Diagnosis of Digital Circuits, Test Generation Techniques for Combinational Circuits, Detection of Multiple Faults in Combinational Logic Circuits. Testable Combinational Logic Circuit Design: The Reed-Mullar Expansion Technique, Three-Level OR-AND-OR Design, Automatic Synthesis of Testing Logic, Testable Design of Multilevel Combinational Circuits, Synthesis of Random Pattern Testable Combinational Circuits, Path Delay Fault Testable Combinational Logic Design, Testable PLA Design.	12
III	Test Generation for Sequential Circuits: Testing of Sequential Circuits as Iterative Combinational Circuits, State Table Verification, Test Generation Based on Circuit Structure, Functional Fault Models, Test Generation Based on Functional Fault Models.	7
IV	Design of Testable Sequential Circuits: Controllability and Observability, Ad Hoc Design Rules for Improving Testability, Design of Diagnosable Sequential Circuits, The Scan-Path Technique for Testable Sequential Circuit Design, Level-Sensitive Scan Design, Random Access Scan Technique, Partial Scan, Testable Sequential Circuit Design Using Nonscan Techniques, Cross Check, Boundary Scan	7
V	Built-In Self-Test: Test Pattern Generation for BIST, Output Response Analysis, Circular BIST, BIST Architectures. Testable Memory Design: RAM Fault Models, Test Algorithms for RAMs, Detection of Pattern Sensitive Faults, BIST Techniques for Ram Chips, Test Generation and BIST for Embedded RAMs.Design verification techniques based on simulation, analytical and formal approaches. Functional verification. Timing verification. Formal verification. Basics of equivalence checking and model checking. Hardware emulation.	6

Text Books:

1. P. K. Lala, "Digital Circuit Testing and Testability", Academic Press.
2. M.L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwar Academic Publishers.
3. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House
   T.Kropf, "Introduction to Formal Hardware Verification", Springer Verlag, 2000.

1. P. Rashinkar, Paterson and L. Singh, "System-on-a-Chip Verification-Methodology and Techniques", Kluwer Academic Publishers, 2001.

Course Outcomes:

CO202.1	apply the concepts in testing which can help them design a better yield in IC design.
CO202.2	tackle the problems associated with testing of semiconductor circuits at earlier design levels so as to significantly reduce the testing costs.
CO202.3	analyse the various test generation methods for static & dynamic CMOS circuits.
CO202.4	identify the design for testability methods for combinational & sequential CMOS circuits.
CO202.5	recognize the BIST techniques for improving testability.

MTMC-251	Advanced VLSI Design Lab	L: 0	T: 0	P: 6	Credits : 2

Course Objective: Students undergoing this course are expected to:

1. Familiar with CADENCE Virtuoso to perform the circuit simulation.
2. To perform the analysis and layout designing of the circuit.
3. Calculate all the performance parameters of the implemented circuits.
4. Perform Monte Carlo and Process corner analysis.

Session-I: VLSI System Design

1. Design/Simulation of other Analog building blocks a.
   a. Comparators
   b. Oscillators
   c. PLLs
   d. Switched capacitor circuits
   e. Noise Analysis
2. Mini Projects involving
   a. Unpipelined MIPS Processor
   b. Pipelined MIPS Processor
   c. Out of Order Execution with Tomasulo's Algorithm
   d. Communication Controllers
   e. Arithmetic Circuits
   f. DSP Systems

Session-II: ASIC Design

Experiments shall be carried out using Microwind/System Crafter Tools

1. Part-I: Backend Design

   a. Schematic Entry/ Simulation / Layout/ DRC/PEX/Post Layout Simulation of
   b. CMOS Inverter,
   c. NAND Gate,
   d. OR Gate,
   e. Flip Flops,
   f. Register Cell,
   g. Half Adder,
   h. Full Adder Circuits

2. Part-II: Semicustom Design

   a. HDL Design Entry/ Logic Simulation,
   b. RTL Logic Synthesis,
   c. Post Synthesis Timing Simulation, Place & Route,
   d. Design for Testability, Static Timing Analysis,
   e. Power Analysis of Medium Scale Combinational, Sequential Circuits

3. Part-III: High Speed/Low Power CMOS Design

   a. Designing combinational/sequential CMOS circuits for High Speed Designing

      combinational/sequential CMOS circuits for Low Power

Course Outcomes:

CO251.1	Familiar with CADENCE Virtuoso to perform the circuit simulation.
CO251.2	To perform the analysis and layout designing of the circuit.
CO251.3	Calculate all the performance parameters of the implemented circuits.
CO251.4	Perform Monte Carlo and Process corner analysis.

MTMC-011	Modeling of Microelectronic Devices	L: 3	T: 1	P: 0	Credits : 3

Course Objectives:

1. Understand the fundamental concepts of semiconductor physics, including energy bands, charge carriers, and the energy band model.
2. Gain knowledge of MOS capacitors, their characteristics, and the principles of biasing MOSFETs.
3. Explore advanced topics related to MOSFETs, compound semiconductor FETs, and their applications in low-voltage and low-power devices.
4. Analyze the behavior of Schottky barriers and ohmic contacts, and understand their DC and small-signal models.
5. Examine the principles of operation and modeling of bipolar junction transistors, including silicon and heterojunction bipolar transistors.

Syllabus:

Unit	Topic	Lectures
I	**Basic Semiconductor Physics:**Energy bands and Charge Carriers: Solid State Electronic materials, Drift Currents in Semiconductors, Covalent Bond and Energy Bands. Energy Band Model and Fermi Level.MOS Capacitor: Characteristics of the MOS Capacitors, NMOS Transistor, PMOS Transistor, Biasing the MOSFET, Capacitances in MOS Transistor.	**8**
II	**MOSFET and Compound Semiconductor FET:**Introduction to Scaled MOSFETs, CMOS / BiCMOS, Reliability, SOI and 3D Structures, Memory Structures, Low-Voltage / Low – Power Devices.GaAs MESFETs, Hetero-structure Field-Effect Transistors, Gate Leakage Current, Novel Compound-Semiconductor FETs.	**8**
III	**Schottky Barriers and Ohmic Contacts:** DC – Current – Voltage Characteristics, Static Model, Large – Signal Model, Small – Signal model.	**8**
IV	**Bipolar Junction Transistors:** Introduction, Principles of Bipolar Transistor Operation, Silicon Bipolar Transistors, Heterojunction Bipolar Transistors, Bipolar Transistor Modelling.	**8**
V	**Recent Developments in Microelectronic Devices:** Introduction, Transit – Time Diodes, Resonant – Tunnelling Diodes, Transferred – Electron Devices.	**8**

TEXT BOOKS:

1. S M Sze, "Modern Semiconductor Device Physics", Wiley 1998.
2. R S Muller and T J Kaminis, "Device Electronics for Integrated Circuits", Second Edition, Wiley 1988.

REFERENCE BOOKS:

1. B G Streetman, "Solid State Electronic Devices", Fourth Edition PH, 1995.
2. D Foty, "MOSFET Modeling with SPICE: Principles and Practices", PH, 1997.
3. P W Tulnenga, "SPICE: A Guide to Circuit Simulation and Analysis using PSPICE", Third Edition, PH, 1995.
4. P Antognetti and C Massobrio, "Semiconductor device and Modeling with SPICE", Third Edition, PH, 1995.
5. T A Fjeidly, T Ytterdai and M Shun, "Introduction to Device Modeling and Circuit Simulation", Wiley, 1997.
6. D Nagachoudhari, "Microelectronic Devices", Pearson 2001.

Course Outcomes:

1. Upon completion of the course, students will be able to explain the concepts of energy bands and charge carriers in solid-state electronic materials.
2. Students will be able to analyze and interpret the characteristics of MOS capacitors and understand the operation of NMOS and PMOS transistors.
3. Students will be able to discuss and compare different types of FETs, including scaled MOSFETs, CMOS/BiCMOS, GaAs MESFETs, and novel compound-semiconductor FETs.
4. Upon completion of the course, students will be able to analyze the behavior of Schottky barriers and ohmic contacts using their DC and small-signal models.
5. Students will be able to demonstrate an understanding of bipolar junction transistors, including their principles of operation, modeling, and the characteristics of silicon and heterojunction bipolar transistors.

MTMC-012	Designing with ASICS	L: 3	T: 1	P: 0	Credits : 3

Course Objective: Students undergoing this course are expected to:

1. Demonstrate in-depth knowledge in ASIC Design flow , ASICs Design styles and issues,
2. ASICs Design Techniques. ASIC construction.
3. Analyze the characteristics and performance of ASICs and judge independently the best suited device for conducting research in ASIC design.
4. Solve problems of Design issues, simulation and Testing of ASICs.
5. Apply appropriate techniques, resources and tools to engineering activities for appropriate solution to develop ASICs

Syllabus:

Unit	Topics	Lectures
I	Types of ASICs -Standard Cell-Gate Arrays, PLD's, Structured Gate Array .ASIC Design Flow , CMOS modeled as Transistor and , Capacitor ,CMOS Design rules – Lamda Based Design Rule, Mead Conway ,Design of Combinational Logic Cell, ,Data Path cell Library architecture.	8
II	ASIC Library Design - Transistors as Resistors, Logical Effort , Transistor Parasitic Capacitance, Drive Strength calculation ,Logical effort - Library cell design programmable ASIC design software: Design system – logic synthesis – half gate ASIC.	8
III	Low level design entry: Schematic entry – low level design languages – PLA tools – EDIF .Problems with Boolean function implementation based on ACTEL & Xilinx FPGA in detail with an example	8
IV	An overview of VHDL and verilog. Logic synthesis in verilog and & VHDL simulation.Implementstion of combinational and sequential circuits	8
V	ASIC Construction –.Constructive Partitioning - Iterative Partitioning ; K-L Algorithm ; Ratio-Cut ; Look-ahead algorithm Placement: Floor planning- Delay Measurement – Channel and I/O power planning - Placement- Min-Cut algorithms in detail ,Physical Design Flow. Routing: Global Routing , Interconnection Mechanism – routing inside flexible bolcks ,Detailed Routing- Left Edge algorithm; Area routing with an example, Special Routing. Clock Routing; Power routing. Circuit ,Extraction & DRC for ASIC design - Design checks	8

Text / References:

1. J.S. Smith, "Application specific Integrated Circuits", Pearson Education, 2008
2. Wayne Wolf, "FPGA-Based System Design", Prentice Hall PTR, 2009.
3. Farzad Nekoogar and Faranak Nekoogar, "From ASICs to SOCs: A Practical Approach", Prentice Hall PTR, 2003.

Course Outcomes:

CO012.1	Demonstrate VLSI tool-flow and appreciate FPGA architecture.
CO012.2	Understand the issues involved in ASIC design, including technology choice, design management, tool-flow, verification, debug and test, as well as the impact of technology scaling on ASIC design.
CO012.3	understand the algorithms used for ASIC construction
CO012.4	Understand the basics of System on Chip, On chip communication architectures like AMBA, AXI and utilizing Platform based design.
CO012.5	Demonstrate and appreciate high performance algorithms available for ASICs

MTMC-013	Low Power VLSI Design	L: 3	T: 1	P: 0	Credits : 3

Course Objectives:

1. Understand the principles and challenges of low-voltage and low-power design in integrated circuits.
2. Gain knowledge of MOS/BiCMOS processes and their integration considerations in low-power design.
3. Explore deep submicron processes, including SOI CMOS and lateral BJT on SOI, and their implications for low-voltage/low-power CMOS/BiCMOS processes.
4. Analyze and model the behavior of advanced MOSFETs and bipolar devices, considering their limitations.
5. Study conventional CMOS and BiCMOS logic gates, evaluate their performance, and compare advanced BiCMOS digital circuits for low-voltage and low-power applications.

Syllabus:

Unit	Topics	Lectures
I	LOW POWER DESIGN, AN OVER VIEW: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.MOS/BiCMOS PROCESSES: Bi-CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES: Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/Bi-CMOS processes.	8
II	DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models, Bipolar models. Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.	8
III	CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS and Bi-CMOS logic gates, Performance Evaluation.	8
IV	LOW- VOLTAGE LOW POWER LOGIC CIRCUITS: Comparison of advanced Bi-CMOS Digital circuits. ESD-free Bi-CMOS, Digital circuit operation and comparative Evaluation.	8
V	LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspectiveSPECIAL TECHNIQUES: Power Reduction in Clock Networks, CMOS Floating Node, Low Power Bus, Delay Balancing, Low Power Techniques for SRAM.	8

Text Books:

1. Yeo Rofail/ Gohl, CMOS/BiCMOS ULSI low voltage, low power, PearsonEducation
2. Gary K. Yeap, Practical Low Power Digital VLSI Design, KAP.
3. Douglas A.Pucknell& Kamran Eshraghian, Basic VLSI Design, PHI Publication.
4. J.Rabaey, Digital Integrated circuits, PHI Publication.
5. Sung-mo Kang and Yusuf Leblebici, CMOS Digital ICs, TMH Publication .
   IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.

Course Outcomes:

1. Upon completion of the course, students will be able to explain the concepts of low-voltage and low-power design, as well as the limitations and benefits associated with it.
2. Students will be able to describe the MOS/BiCMOS processes and understand the integration and isolation considerations in low-power design.
3. Students will be able to analyze the characteristics of deep submicron processes, SOI CMOS, and lateral BJT on SOI, and discuss the future trends in CMOS/BiCMOS processes.

4. Upon completion of the course, students will be able to apply advanced MOSFET and bipolar models, and understand the limitations associated with them.
5. Students will be able to evaluate the performance of conventional CMOS and BiCMOS logic gates, as well as compare advanced BiCMOS digital circuits for low-voltage and low-power applications.

MTMC-014	Nano Technology	L: 3	T: 1	P: 0	Credits : 3

Course Objectives:

1. Understand the fundamental concepts of nano-scale systems, including length, energy, and time scales.
2. Explore different lithography techniques for nano-scale fabrication, such as optical, deep ultraviolet, X-ray, electron beam, and ion beam lithography.
3. Study the behavior of single electron transistors and the coulomb blockade effects in ultra-small metallic tunnel junctions.
4. Gain knowledge of quantum mechanics in the context of nanostructures, including quantum confinement in semiconductor nanostructures, band gap engineering, and the Landauer-Büttiker formalism.
5. Learn about molecular techniques in nano-scale systems, including molecular electronics, chemical self-assembly, carbon nanotubes, self-assembled monolayers, and electromechanical techniques.

Syllabus:

Unit	Topic	Lectures
1.	**Introduction** to nano scale systems, Length energy and time scales, Top down approach to Nano lithography, Spatial resolution of optical, deep ultraviolet, X-ray, electron beam and ion beam lithography, Single electron transistors, coulomb blockade effects in ultra small metallic tunnel junctions.	8
2.	**Quantum Mechanics** Quantum confinement of electrons in semiconductor nano structures, Two dimensional confinement (Quantum wells), Band gap engineering, Epitaxy, Landaeur – Buttiker formalism for conduction in confined geometries,	8
3.	**One Dimensional Confinement**, Quantum point contacts, quantum dots and Bottom up approach, Introduction to quantum methods for information processing.	8
4.	**Molecular Techniques** Molecular Electronics, Chemical self assembly, carbon nano tubes, Self assembled mono layers, Electromechanical techniques,	8
5.	**Applications** in biological and chemical detection, Atomic scale characterization techniques, scanning tunnelling microscopy, atomic force microscopy	8

TEXT BOOKS:

1. Beenaker and Van Houten "Quantum Transport in Semiconductor Nanostructures in Solid state Physics" Ehernreich and Turnbell, Academic press, 1991.

REFERENCE BOOKS:

1. David Ferry "Transport in Nano structures" Cambridge University press 2000.
2. Y. Imry "Introduction to Mesoscopic Physics, Oxford University press 1997.
3. S. Dutta "Electron Transport in Mesoscopic systems" Cambridge University press 1995.
4. H Grabert and M Devoret "Single charge Tunneling" Plenum press 1992.

Course Outcomes:

1. Upon completion of the course, students will be able to explain the principles and significance of nano-scale systems and their length, energy, and time scales.
2. Students will be able to compare and analyze different lithography techniques for nano-scale fabrication, considering their spatial resolution and limitations.
3. Students will be able to analyze and understand the behavior of single electron transistors and the coulomb blockade effects in ultra-small metallic tunnel junctions.
4. Upon completion of the course, students will be able to apply quantum mechanics concepts to explain quantum confinement in semiconductor nanostructures, band gap engineering, and the Landauer-Büttiker formalism for conduction in confined geometries.
5. Students will be able to describe and evaluate molecular techniques in nano-scale systems, including molecular electronics, chemical self-assembly, carbon nanotubes, self-assembled monolayers, and electromechanical techniques

MTMC-021	Advanced Embedded Systems	L: 3	T: 1	P: 0	Credits : 3

Course Objectives:

1. Understand the components and architecture of typical embedded systems, including the core, memory, sensors and actuators, communication interface, embedded firmware, and other system components.
2. Explore the characteristics and quality attributes of embedded systems, including hardware-software co-design, program modeling, and the use of Unified Modeling Language (UML) in embedded design.
3. Gain knowledge of embedded hardware design and development, including the use of Electronic Design Automation (EDA) tools for schematic design, PCB layout design, and netlist creation.
4. Study the architecture and programming features of the ARM Cortex M3 32-bit microcontroller family, including the use of general-purpose registers, interrupt controllers, and memory protection.
5. Learn about embedded firmware design approaches, development languages, and the role of real-time operating systems (RTOS) in embedded system design, including task scheduling, communication, synchronization, and device drivers.

Syllabus:

Unit	Topics	Lectures
I	**Typical Embedded System:** Core of the Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware,Other System Components. **Characteristics and Quality Attributes of Embedded Systems:** Hardware Software Co-Design and Program Modeling: Fundamental Issues inHardware Software Co-Design, Computational Models in Embedded Design, Introduction to Unified Modeling Language, Hardware SoftwareTrade-offs.	8
II	**Embedded Hardware Design and Development** :EDA Tools, How to Use EDA Tool, Schematic Design – Place wire, Bus , port, junction,creating part numbers, Design Rules check, Bill of materials, Netlist creation , PCB Layout Design – Building blocks, Component placement,PCB track routing.	8
III	**ARM -32 bit Microcontroller family.** Architecture of ARM Cortex M3 –General Purpose Registers, Stack Pointer, Link Register, ProgramCounter, Special Register,.Nested Vector Interrupt Controller. Interrupt behavior of ARM Cortex M3. Exceptions Programming. AdvancedProgramming Features.Memory Protection. Debug Architecture.	8
IV	**Embedded Firmware Design and Development:** Embedded Firmware Design Approaches, Embedded Firmware Development Languages **Real-Time Operating System (RTOS) based Embedded System Design**: Operating System Basics, Types of OS, Tasks, Process and Threads,Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, TaskSynchronization, Device Drivers, How to Choose an RTOS.	8
V	**The Embedded System Development Environment**: The Integrated Development Environment (IDE), Types of Files Generated on Crosscompilation, Disassembler/ELDompiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan.	8

Text Books:

1. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Ltd
2. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", Newnes, (Elsevier).

James K Peckol, "Embedded Systems – A contemporary Design Tool", John Weily& Sons.

Course Outcomes:

1. Upon completion of the course, students will be able to identify and describe the core components and architecture of typical embedded systems.
2. Students will be able to analyze the characteristics and quality attributes of embedded systems and understand the importance of hardware-software co-design and program modeling.
3. Students will be able to use EDA tools for schematic design and PCB layout design, and generate netlists and bill of materials for embedded hardware development.
4. Upon completion of the course, students will be able to explain the architecture and programming features of the ARM Cortex M3 microcontroller family, including interrupt handling and memory protection.
5. Students will be able to design and develop embedded firmware using appropriate approaches and development languages, and understand the role of an RTOS in task scheduling, communication, synchronization, and device driver implementation.

MTMC-021	CMOS RF Design	L: 3	T: 1	P: 0	Credits : 3

Course Objectives:

1. Understand the fundamental concepts of RF design and wireless technology, including the complexity and choice of technology in RF design applications.
2. Study the basic concepts in RF design, such as nonlinearity, time variance, inter-symbol interference, random processes, noise, sensitivity, dynamic range, and gains and distortion conversions.
3. Explore analog and digital modulation techniques for RF circuits, including power efficiency comparisons, coherent and non-coherent detection, and basics of multiple access techniques.
4. Learn about RF testing methodologies for different types of receivers, including heterodyne, homodyne, image reject, direct IF, and sub-sampled receivers.
5. Study the behavior of BJT and MOSFET devices at RF frequencies, including modeling, SPICE models, noise performance, integrated parasitic elements, and their monolithic implementation.

Syllabus:

Unit	Topic	Lectures
I	**Introduction to RF design** and Wireless Technology: Design and Applications, Complexity and Choice of Technology. Basic concepts in RF design: Nonlinearly and Time Variance, Inter-symbol interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion.	**8**
II	**RF Modulation**: Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection, Mobile RF communication and basics of Multiple Access techniques. Receiver and Transmitter architectures. Direct conversion and two-step transmitters.	**8**
III	**RF Testing**: RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.	**8**
IV	**BJT and MOSFET Behavior at RF Frequencies**: BJT and MOSFET behavior at RF frequencies, Modeling of the transistors and SPICE model, Noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation	**8**
V	**RF Circuits Design:** Overview of RF Filter design, Active RF components & modeling, Matching and Biasing Networks. Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, Various mixers- working and implementation. Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design, Liberalization techniques, Design issues in integrated RF filters.	**8**

TEXT BOOKS:

1. Ludwig R, Bretchko P, "RF Circuits Design", Pearson 2000 Ed
2. Thomas H. Lee "Design of CMOS RF Integrated Circuits" Cambridge University press 1998.

REFERENCE BOOKS:

1. B Razavi "RF Microelectronics" PHI 1998
2. R Jacob Baker, H W Li, D E Boyce " CMOS Circuit Design, layout and Simulation" PHI 1998
3. Y P Tsividis "Mixed Analog and Digital Devices and Technology" TMH 1996

Course Outcomes:

1. Upon completion of the course, students will be able to explain the design and application aspects of RF design and wireless technology, considering the complexity and choice of technology.
2. Students will be able to analyze and mitigate nonlinearity, time variance, inter-symbol interference, random processes, and noise in RF design.
3. Students will be able to compare and apply different modulation techniques for RF circuits, considering power efficiency, detection methods, and multiple access techniques.
4. Upon completion of the course, students will be able to perform RF testing for various receiver architectures and understand the specific testing requirements for different types of receivers.
5. Students will be able to analyze the behavior of BJT and MOSFET devices at RF frequencies, model their characteristics using SPICE models, consider noise performance and limitations, and understand the impact of integrated parasitic elements.

MTMC-023	VLSI Technology	L: 3	T: 1	P: 0	Credits : 3

Course Objective: Students undergoing this course are expected to:

1. To understand the concepts of MOS transistors operations and their wafer cleaning process
2. To know the fabrication process of CMOS technology and its various kinetics of Silicon dioxide growth design rules.
3. To know the concepts of Failure mechanisms in metal interconnects
4. To learn about the VLSI Plasma and Rapid Thermal Processing
5. To study the concepts of process integration for NMOS, CMOS and Bipolar circuits.

Syllabus:

Unit	Topics	Lectures
I	Environment for VLSI Technology: Clean room and safety requirements. Wafer cleaning processes and wet chemical etching techniques. Impurity incorporation: Solid State diffusion modeling and technology; Ion Implantation modeling, technology and damage annealing; characterization of Impurity profiles.	8
II	Oxidation: Kinetics of Silicon dioxide growth both for thick, thin and ultra thin films. Oxidation technologies in VLSI and ULSI; Characterisation of oxide films; High k and low k dielectrics for ULSI. Lithography : Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI; Mask generation.	12
III	Chemical Vapour Deposition techniques: CVD techniques for deposition of poly silicon, silicon dioxide, silicon nitride and metal films; Epitaxial growth of silicon; modeling and technology. Metal film deposition: Evaporation and sputtering techniques. Failure mechanisms in metal interconnects; Multi-level metallization schemes.	8
IV	Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI.	6
V	Process integration for NMOS, CMOS and Bipolar circuits; Advanced MOS technologies.	6

Texts/References

1. C.Y. Chang and S.M.Sze (Ed), "ULSI Technology," McGraw Hill Companies Inc, 1996.
2. S.K. Ghandhi, "VLSI Fabrication Principles," John Wiley Inc., New York, 1983.
3. S.M. Sze (Ed), "VLSI Technology, "2nd Edition, McGraw Hill, 1988.

Course Outcomes:

CO023.1	Recall the basic basics of MOSFET device physics and its wafer operation
CO023.2	Understand the various operations of fabrication process of CMOS technology
CO023.3	Understand the concept of Evaporation and sputtering techniques.
CO023.4	Design the principles of PECVD, Plasma etching and RIE techniques
CO023.5	Understand the concept of advanced MOS technologies

MTMC-024	FPGA Architecture & Applications	L: 3	T: 1	P: 0	Credits : 3

Course Objectives:

1. Understand the concepts, features, and applications of programmable logic devices such as ROM, PLA, PAL, PLD, PGA, CPLD, and FPGA.
2. Gain knowledge of complex programmable logic devices, including Altera series (Max 5000/7000 series and Altera FLEX logic–10000 series CPLD), AMD's CPLD (Mach 1 to 5), Cypress FLASH 370, and Lattice PLST's architectures (3000 series).
3. Study the architecture, design flow, and technology mapping for FPGAs (Field Programmable Gate Arrays).
4. Explore case studies of specific FPGA devices, including Xilinx XC4000, Altera's FLEX 8000/10000 FPGAs, AT&T ORCA's (Optimized Reconfigurable Cell Array), and Actel's ACT-1,2,3.
5. Learn about finite state machines (FSM), including top-down design, state transition tables, state assignments, realization with PAL, alternative realizations, and the use of Petrinets for state machines.

Syllabus:

Unit	Topics	Lectures
I	Programmable Logic ROM, PLA, PAL, PLD, PGA–Features, programming and applications using complex programmable logic devices Altera series–Max 5000/7000 series and Altera FLEX logic–10000 series CPLD, AMD's–CPLD (Mach 1 to 5); Cypress FLASH 370 Device Technology, Lattice PLST's Architectures–3000 Series–Speed Performance and in system programmability.	8
II	FPGAs Field Programmable Gate Arrays–Logic blocks, routing architecture, Design flow, Technology Mapping for FPGAs.Case Studies Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT &T–ORCA's (Optimized Reconfigurable Cell Array): ACTEL's–ACT-1,2,3 and their speed performance.	8
III	Finite State Machines (FSM)-I Top-down Design–State Transition Table, state assignments for FPGAs,Problem of initial state assignmentfor one hot encoding. Derivations of state machine charges. Realization of state machine charts with a PAL.	8
IV	Finite State Machines (FSM)-IIAlternative realization for state machine chart using microprogramming.Linked state machines,One–Hot statemachine, Petrinetes for statemachines–basic concepts, properties, Extended petrinetes for parallelcontrollers. Finite State Machine–Case Study, Meta Stability,Synchronization.	8
V	FSM Architectures and Systems Level Design Architectures centered around non-registered PLDs,State machine designs centered around shift registers,One –Hot design method,Use of ASMs in One –Hot design. K Application of One –Hot method, System level design controller, data path and functional partition.	8

Reference Books:

1. P.K.Chan& S. Mourad, Digital Design using Field ProgrammableGate Array, Prentice Hall.
2. S.Trimberger, Edr., Field Programmable Gate Array Technology,Kluwer Academic Pub.
3. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley& Sons, Newyork.
4. S.Brown,R.Francis, J.Rose, Z.Vransic, Field Programmable GateArray,Kluwer Pub.
5. Richard FJinder , "Engineering Digital Design,"Academic press

Course Outcomes:

1. Upon completion of the course, students will be able to describe the features and programming methods of programmable logic devices and understand their applications.
2. Students will be able to compare and analyze different complex programmable logic devices from Altera, AMD, Cypress, and Lattice and understand their respective architectures, performance, and programmability.

3. Students will be able to apply the design flow and technology mapping techniques for FPGA-based designs.
4. Upon completion of the course, students will be able to analyze and evaluate case studies of specific FPGA devices, including Xilinx, Altera, AT&T ORCA, and Actel, and understand their performance characteristics.
5. Students will be able to design and implement finite state machines using top-down design approaches, state transition tables, PAL realization, alternative realizations, and Petrinets.

MTMC-031	Advanced Microcontrollers and Systems	L: 3	T: 1	P: 0	Credits : 3

Course Objective: After completion of this course student will be able to:

1. Understand the importance of low power embedded systems, low power RF capabilities and applications of microcontroller
2. Knowledge about types of low power microcontrollers, architectures and usage
3. Knowledge about the MSP430 microcontroller and its working
4. Understand the working ARM Cortex-M3 microcontroller and its architecture

Syllabus:

Unit	Topics	Lectures
I	**Motivation for advanced microcontrollers** – Low Power embedded systems, On-chip peripherals, low-power RF capabilities. Applications of Microcontrollers.	8
II	**MSP430 – 16-bit Microcontroller family**. CPU architecture, Instruction set, Interrupt mechanism, Clock system, Memory subsystem, bus – architecture. The assembly language and „C programming for MSP-430 microcontrollers	8
III	**MSP430 – 16-bit Microcontroller Peripherals-** On -chip peripherals. WDT, Comparator, Op-Amp, Timer, Basic Timer, Real Time Clock (RTC), ADC, DAC, Digital I/O. Using the low-power features of MSP430. Clock system, low-power modes, Clock request feature, Low-power programming and interrupts.	8
IV	**ARM -32 bit Microcontroller family.** Architecture of ARM Cortex M3 – General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Register,. Nested Vector Interrupt Controller. Interrupt behavior of ARM Cortex M3. Exceptions Programming.Advanced Programming Features.Memory Protection. Debug Architecture.	8
V	**Applications** – Wireless Sensor Networking with MSP430 and Low-Power RF circuits; Pulse Width Modulation(PWM) in Power Supplies.	8

Reference Books:

1. Joseph Yiu, " The Definitive Guide to the ARM Cortex-M3, , Newnes, (Elsevier).
2. John Davies, " MSP430Microcontorller Basics",Newnes (Elsevier Science).
3. MSP430 Teaching CD-ROM, Texas Instruments.

Course Outcomes:

CO031.1	To develop the understanding of the importance of low power embedded systems, low power RF capabilities and applications of microcontroller
CO031.2	Understanding and applying of MSP430 microcontroller architecture, memory, Real Time Clock, ADC, DAC and low power features
CO031.3	Understanding and applying of ARM Cortex-M3 microcontroller architecture, memory, Interrupt behaviour, exceptions programming
CO031.4	To understand the uses of microcontroller in Wireless sensor Networking with MSP430, Low power RF circuits, Pulse width modulation in power supplies

MTMC-032	Analog Signal Processing	L: 3	T: 1	P: 0	Credits : 3

Course Objectives:

1. Understand the principles of translinear circuits and their applications, including squarer, divider, square rooting, vector magnitude circuits, and multipliers.
2. Study MOS analog integrated circuits and their basic building blocks, such as the differential amplifier pair, current mirrors, active loads, level shifters, and differential to single-ended converters.
3. Explore low voltage signal processing and the design considerations for CMOS op-amps, including input stages, output stages, frequency response, and slew rate.
4. Learn about current-mode signal processing and its advantages over voltage-mode signal processing, including continuous-time signal processing, current conveyors, current feedback, and their applications.
5. Study selected recent topics in the field, such as the realization of MOS resistors in MOS technology, N-MOS OTA, CMOS OTA, MOSFET-C circuits, and CMOS transconductor circuits.

Syllabus:

Unit	Topics	Lectures
I	Translinear Bipolar and MOS Circuits: General Translinear principles , various translinear circuits: squarer, divider, square rooting, vector magnitude circuit, multipliers, translinear multiplier etc.	8
II	MOS Analog Integrated Circuits: Basic building blocks, differential amplifier pair, various current mirrors, active loads, level shifter, differential to single ended converter, complete N-MOS Op-amp.	8
II	Low Voltage Signal Processing: Need of low voltage signal processing, C-MOS Op-amp design: input stages, output stages, frequency response, slew rate etc., BI-CMOS op-amp design, input stages, out put stages, introduction to low voltage filter filters.	8
IV	Current-Mode Signal Processing: Current-mode compared to voltage mode, continuous time signal processing, current conveyors and their applications, current feedback and its applications.	8
V	Selected Recent Topics: Realization of MOS resistors in MOS technology, N-MOS OTA, C-MOS OTA, MOSFET-C and other related circuits, C-MOS transconductor circuits.	8

Text/References

1. C.Toumazou, F.J. Lidgey and D.G.Haigh, 'Analog IC design: The current-mode approach', Exeter, England: Peter Peregrinus, 1990.
2. M. Ismail and T. Fiez, 'Analog VLSI: Signal and Information Processing', Mc Graw Hill, 1994.
3. B. Razavi, 'Design of Analog CMOS Integrated Circuits', Mc Graw Hill, 2000.
4. A.B.Grebene, ' Bipolar and MOS Analog Integrated Circuit Design', Wiley, 1984.
5. A.S.Sedra and K.C.Smith, ' Microelectronic circuits', Oxford University Press.

Course Outcomes:

1. Upon completion of the course, students will be able to analyze and design various translinear circuits, including squarers, dividers, square rooters, vector magnitude circuits, and multipliers.
2. Students will be able to analyze and design MOS analog integrated circuits, including differential amplifier pairs, current mirrors, active loads, level shifters, and differential to single-ended converters.
3. Upon completion of the course, students will be able to design low voltage signal processing circuits, including CMOS op-amps with considerations for input stages, output stages, frequency response, and slew rate.
4. Students will be able to compare and evaluate current-mode signal processing techniques and their advantages over voltage-mode signal processing, and apply current conveyors and current feedback in relevant applications.
5. Students will be able to analyze and design circuits based on selected recent topics, such as MOS resistors, OTA circuits, MOSFET-C circuits, and CMOS transconductor circuits.

MTMC-033	Analog IC Design	L: 3	T: 1	P: 0	Credits : 3

Course Objective: Students undergoing this course are expected to:

1. To introduce the basic analog circuits to get familiar with the small and large-signal models of CMOS transistors.
2. Understand the various single stage amplifiers.
3. Understand the Qualitative Analysis and Quantitative Analysis of MOS differential pair.
4. Gain the knowledge of frequency response compensations & stability of operational amplifier..
5. Understand the general considerations like power supply rejection, stability and other compensation techniques.

Syllabus:

Unit	Topics	Lectures
I	**Basic MOS Device Physics:** General Considerations, MOSFET as a Switch, MOSFET Structure, MOS Symbols, MOS I/V Characteristics, Threshold Voltage, Derivation of I/V Characteristics, Second-Order Effects, MOS Device Models, MOS Device Layout, MOS Device Capacitances, MOS Small-Signal Model, MOS SPICE models, NMOS versus PMOS Devices, Long-Channel versus Short-Channel Devices.	7
II	**Single-Stage Amplifiers,** Basic Concepts , Common-Source Stage, Common-Source Stage with Resistive Load ,CS Stage with Diode-Connected Load, CS Stage with Current-Source Load, CS Stage with Triode Load, CS Stage with Source Degeneration, Source Follower, Common-Gate Stage, Cascode Stage, Folded Cascode, Choice of Device Models.	7
III	**Differential Amplifiers,** Single-Ended and Differential Operation. Basic Differential Pair, Qualitative Analysis, Quantitative Analysis, Common-Mode Response, Differential Pair with MOS Loads, Gilbert Cell, Passive and Active Current Mirrors, Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors, Large-Signal Analysis, Small-Signal Analysis, Common-Mode Properties	8
IV	**Frequency Response of Amplifiers,** General Considerations, Miller Effect, Association of Poles with Nodes, Common-Source Stage, Source Followers, Common-Gate Stage, Cascode Stage, Differential Pair **Feedback** General Considerations, Properties of Feedback Circuits, Types of Amplifiers, Feedback Topologies, Voltage-Voltage Feedback, Current-Voltage Feedback, Voltage-Current Feedback, Current-Current Feedback, Effect of Loading, Two-Port Network Models, Loading in Voltage-Voltage Feedback, Loading in Current-Voltage Feedback, Loading in Voltage-Current Feedback, Loading in Current-Current Feedback, Summary of Loading Effects, Effect of Feedback on Noise	10
V	**Operational Amplifiers**, General Considerations , Performance Parameters, One-Stage Op Amps, Two-Stage Op Amps , Gain Boosting , Comparison , Common-Mode Feedback . Input Range Limitations, Slew Rate, Power Supply Rejection. Stability and Frequency Compensation General Considerations, Multipole Systems, Phase Margin, Frequency Compensation, Compensation of Two-Stage Op Amps, Slewing in Two-Stage Op Amps, Other Compensation Techniques.	8

Reference Books:

1. B. Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill Publications/
2. P. R. Gray & R. G. Meyer, “Analysis and Design of Analog Integrated Circuits”, John Wiley Publications.
3. R. Gregorian and Temes, “Analog MOS Intgrated Circuits for Signal Processing”, Wiley Publications.
4. Ken Martin, “Analog Integrated Circuit Design”, Wiley Publications.
5. Sedra and Smith, “Microelectronic Circuits”, Oxford Publications.
6. B.Razavi, “Fundamentals of Microelectronics”, Wiley Publications.

Course Outcomes:

CO033.1	Recall the basic basic analog circuits to provide a foundation for advanced designs
CO033.2	.Understand characteristics of single stage amplifier using CMOS
CO033.3	Analysing the various CMOS Analog and Mixed signal Circuits.
CO033.4	Design feedback topologies and loading effects.
CO033.5	Understand the general considerations like power supply rejection, stability and other compensation techniques.

MTMC-041	Hardware Description Languages	L: 3	T: 1	P: 0	Credits : 3

Course Objectives:

1. Understand the fundamentals of hardware modeling using the Verilog HDL, including hardware encapsulation, descriptive styles, structural connections, and behavioral descriptions.
2. Study logic systems, data types, and operators for modeling in Verilog HDL, including user-defined primitives, variables, data types, constants, operators, and expressions.
3. Explore behavioral descriptions in Verilog HDL, including procedural assignments, timing controls, tasks, functions, and behavioral models of finite state machines.
4. Learn about the synthesis of combinational logic using HDL-based synthesis methodologies, technology-independent design, technology mapping, shared resources, and synthesis of sequential logic.
5. Study the synthesis of language constructs, including nets, register variables, expressions, assignments, case and conditional statements, loops, and user-defined tasks and functions.

Syllabus:

Unit	Topics	Lectures
I	HARDWARE MODELING WITH THE VERILOG HDL : Hardware Encapsulation –TheVerilog Module, Hardware Modeling Verilog Primitives, Descriptive Styles, StructuralConnections, Behavioral Description In Verilog, Hierarchical Descriptions of Hardware,Structured (Top Down) Design Methodology, Arrays of Instances, Using Verilog for Synthesis,Language Conventions, Representation of Numbers.LOGIC SYSTEM, DATA TYPES AND OPERATORS FOR MODELING IN VERILOGHDL: User-Defined Primitives, User Defined Primitives – Combinational Behavior User-DefinedPrimitives –Sequential Behavior, Initialization of Sequential Primitives. Verilog Variables, LogicValue Set, Data Types, Strings. Constants, Operators, Expressions and Operands, OperatorPrecedence Models Of Propagation Delay; Built-In Constructs for Delay, Signal Transitions,	8
II	BEHAVIORAL DESCRIPTIONS IN VERILOG HDL: Verilog Behaviors, BehavioralStatements, Procedural Assignment, Procedural Continuous Assignments, Procedural TimingControls and Synchronization, Intra-Assignment, Delay-Blocked Assignments, Non-BlockingAssignment, Intra-Assignment Delay: Non-Blocking Assignment, Simulation of SimultaneousProcedural Assignments, Repeated Intra Assignment Delay, Indeterminate Assignments andAmbiguity, Constructs for Activity Flow Control, Tasks and Functions, Summary of DelayConstructs in Verilog, System Tasks for Timing Checks, Variable Scope Revisited, ModuleContents, Behavioral Models of Finite State Machines.	8
III	SYNTHESIS OF COMBINATIONAL LOGIC: HDL-Based Synthesis, Technology-Independent Design, Benefits of Synthesis, Synthesis Methodology, Vendor Support, Styles forSynthesis of Combinational Logic, Technology Mapping and Shared Resources, Three StateBuffers, Three State Outputs and Don t Cares, Synthesis of Sequential Logic Synthesis ofSequential Udps, Synthesis of Latches, Synthesis of Edge-Triggered Flip Flops, RegisteredCombinational Logic, Shift Registers and Counters, Synthesis of Finite State Machines, Resets,Synthesis of Gated Clocks, Design Partitions and Hierarchical Structures.	8
IV	INTRODUCTION TO VHDL: An Overview of Design Procedures used for System Designusing CAD Tools. Design Entry. Synthesis, Simulation, Optimization, Place and Route. DesignVerification Tools. Examples using Commercial PC Based on VHDL Elements of VHDL TopDown Design with VHDL Subprograms. Controller Description VHDL Operators.	8
V	**BEHAVIORAL DESCRIPTION OF HARDWARE IN VHDL:** Process Statement AssertionStatements, Sequential Wait Statements Formatted ASCII I/O Operators, MSI-Based Design.Differences between VHDL and Verilog.	8

Reference Books:

1. M.D.CILETTI, Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice-Hall.

2. Z.NAWABI, VHDL Analysis and Modeling of Digital Systems, McGraw Hill.
3. M.G.ARNOLD, Verilog Digital – Computer Design", Prentice-Hall (PTR).
4. PERRY, "VHDL", McGraw Hill.

Course Outcomes:

1. Upon completion of the course, students will be able to effectively use the Verilog HDL for hardware modeling, including encapsulating hardware, using descriptive styles, and creating hierarchical designs.
2. Students will be able to apply the appropriate logic systems, data types, and operators in Verilog HDL to model hardware behavior accurately.
3. Upon completion of the course, students will be able to write behavioral descriptions in Verilog HDL, including procedural assignments, timing controls, and behavioral models of finite state machines.
4. Students will be able to synthesize combinational and sequential logic using HDL-based synthesis methodologies, considering technology-independent design, technology mapping, and synthesis of finite state machines.
5. Upon completion of the course, students will be able to synthesize language constructs in Verilog HDL, including nets, register variables, expressions, assignments, control statements, loops, and user-defined tasks and functions.

MTMC 042	Advanced Computer Architecture	L: 3	T: 1	P: 0	Credits : 3

Course Objectives:

1. Understand the different parallel computer models and their classification, including multiprocessors, multi-computers, multi-vector, and SIMD computers.
2. Study the properties of parallel programs and networks, including conditions of parallelism, data and resource dependences, program partitioning and scheduling, program flow mechanisms, and comparisons of flow mechanisms.
3. Explore system interconnect architectures, including network properties, routing, static and dynamic interconnection networks, multiprocessor system interconnects, hierarchical bus systems, crossbar switches, and multistage networks.
4. Learn about advanced processors, including advanced processor technology, instruction-set architectures, CISC and RISC scalar processors, superscalar processors, VLIW architectures, and vector and symbolic processors.
5. Study pipeline design principles, including linear and nonlinear pipeline processors, instruction pipeline design, dynamic instruction scheduling, branch handling techniques, arithmetic pipeline design, computer arithmetic principles, and multifunctional arithmetic pipelines.

Syllabus:

Unit	Topics	Lectures
I	Parallel computer models: The state of computing, Classification of parallel computers, Multiprocessors and multi computers, Multi vector and SIMD computers. Program and network properties: Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms	8
II	System Interconnect Architectures: Network properties and routing, Static interconnection Networks, Dynamic interconnection Networks, Multiprocessor system Interconnects, Hierarchical bus systems, Crossbar switch and multiport memory, Multistage and combining network.Advanced processors: Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Vector and Symbolic processors	8
III	Pipelining: Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multifunctional arithmetic pipelines	8
IV	Memory Hierarchy Design: Cache basics & cache performance, reducing miss rate and miss penalty, multilevel cache hierarchies, main memory organizations, design of memory hierarchies.	8
V	Multiprocessor architectures: Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, MOESI), scalable cache coherence, overview of directory based approaches, design challenges of directory protocols, memory based directory protocols, cache based directory protocols, protocol design tradeoffs, synchronization,	8

Texts

1. Kai Hwang, “Advanced Computer architecture”; TMH.
2. Advance Microprocessor Senthile Oxford

References

3. D. A. Patterson and J. L. Hennessey, “Computer organization and design,” Morgan Kaufmann, 2nd Ed.
4. J.P.Hayes, “computer Architecture and organization”; MGH.
5. Harvey G.Cragon,”Memory System and Pipelined processors”; Narosa Publication.

6. V.Rajaranam & C.S.R.Murthy, “Parallel computer”; PHI.
7. R.K.Ghose, Rajan Moona & Phalguni Gupta, “Foundation of Parallel Processing”; Narosa Publications.
8. Kai Hwang and Zu, “Scalable Parallel Computers Architecture”; MGH.

Course Outcomes:

1. Upon completion of the course, students will be able to classify and analyze different parallel computer models and understand their characteristics and applications.
2. Students will be able to identify and analyze the properties of parallel programs and networks, including conditions of parallelism, dependences, and program flow mechanisms.
3. Upon completion of the course, students will be able to analyze and design system interconnect architectures, considering network properties, routing, and different interconnection techniques.
4. Students will be able to evaluate and compare advanced processor technologies and architectures, including CISC, RISC, superscalar, VLIW, and vector processors.
5. Upon completion of the course, students will be able to design and analyze pipeline processors, including instruction pipeline design, dynamic instruction scheduling, branch handling techniques, and arithmetic pipeline design.

MTMC 043	DIGITAL IC DESIGN	L: 3	T: 1	P: 0	Credits : 3

Course Objective: Students undergoing this course are expected to:

1. To understand the issues and quality metrics of digital design
2. To apply the mixed logic design notation.
3. To study various problems and characteristics of CMOS inverter
4. To study digital circuits using various logic combinational circuits and their limitations.
5. To highlight the sequential circuit design issues in the context of VLSI technology.

Syllabus:

Unit	Topics	Lectures
I	Introduction: Historical Perspective, Issues in Digital Integrated Circuit Design,Quality Metrics of a Digital Design - Cost of an Integrated Circuit, Functionality and Robustness, Performance, Power and Energy Consumption – The Manufacturing Process -Introduction, Manufacturing CMOS Integrated Circuits, The Silicon Wafer, Photolithography, Some Recurring Process Steps Simplified CMOS Process Flow, Design Rules — The Contract between Designer and Process Engineer	8
II	Devices: Introduction, The Diode, A First Glance at the Diode — The Depletion Region, Static Behavior, Dynamic, or Transient, Behavior, The Actual Diode—Secondary Effects, The SPICE Diode Model, The MOS(FET) Transistor, A First Glance at the Device, The MOS Transistor under Static Conditions, Dynamic Behavior, The Actual MOS Transistor— Some Secondary Effects, SPICE Models for the MOS Transistor – Wire: Introduction, A First Glance, Interconnect Parameters — Capacitance, Resistance, and Inductance, Capacitance, Resistance, Inductance	8
III	The CMOS Inverter: Introduction, The Static CMOS Inverter — An Intuitive Perspective, Evaluating the Robustness of the CMOS Inverter: The Static Behavior, Switching Threshold, Noise Margins, Robustness Revisited, Performance of CMOS Inverter: The Dynamic Behavior, Computing the Capacitances, Propagation Delay: First-Order Analysis, Propagation Delay from a Design Perspective, Power, Energy, and Energy-Delay, Dynamic Power Consumption, Static Consumption, Perspective: Technology Scaling and its Impact on the Inverter Metrics	8
IV	Designing Combinational Logic Gates in CMOS: Introduction, Static CMOS Design, Complementary CMOS, Ratioed Logic, Pass-Transistor Logic, Dynamic CMOS Design, Dynamic Logic: Basic Principles, Speed and Power Dissipation of Dynamic Logic, Issues in Dynamic Design, Cascading Dynamic Gates, Perspectives, How to Choose a Logic Style, Designing Logic for Reduced Supply Voltages	8
V	Designing Sequential Logic Circuits: Introduction, Timing Metrics for SequentialCircuits, Classification of Memory Elements, Static Latches and Registers, The Bistability Principle, Multiplexer-Based Latches Master-Slave Edge-Triggered Register, Low-Voltage Static Latches, Static SR Flip-Flops—Writing Data by Pure Force, Dynamic Latches and Registers, Dynamic Transmission-Gate Edge-triggered Registers C2MOS—A Clock-Skew Insensitive Approach, True Single-Phase Clocked Register (TSPCR), Pipelining: An approach to optimize sequential circuits, Latch- vs. Register-Based Pipelines, NORA-CMOS—A Logic Style for Pipelined Structures, Non-Bistable Sequential Circuits, The Schmitt Trigger, Monostable Sequential Circuits, Astable Circuits, Perspective: Choosing a Clocking Strategy	8

Reference Books:

1. Jan M. RabaeyAnanthaChandrakasan, &BorivojeNikolic, “Digital Integrated Circuits – A design perspective”, PHI Publication.
2. S. M. Kang & Y. Leblebici, “CMOS Digital Integrated Circuits”, McGraw Hill Publication.
3. Jackson & Hodges, “Analysis and Design of Digital Integrated circuits”,. TMH Publication.
4. Ken Martin, “Digital Integrated Circuit Design”, Oxford Publications.

5. Sedra and Smith, "Microelectronic Circuits" Oxford Publications.

Course Outcomes:

CO043.1	Recall issues and quality metrics of digital design.
CO043.2	Implementation of mixed logic for circuit design.
CO043.3	Solve problems regarding CMOS inverter Noise margin , power and timing.
CO043.4	Design the combinational and sequential logic circuits and construct circuit timing parameters.
CO043.5	Summarize the concept of sequential circuits and Physical VLSI system design; floor planning, data and control path.

MTMC 044	Advanced Communications Network	L: 3	T: 1	P: 0	Credits : 3

Course Objectives:

1. Understand the concepts, challenges, and history of the Internet, including high-speed networks like ATM.
2. Study TCP/IP congestion and flow control mechanisms in the Internet, analyzing throughput, fairness, and performance for high-bandwidth delay networks.
3. Explore real-time communications over the Internet, adaptive applications, latency and throughput issues, and the integrated services model (intServ) for resource reservation.
4. Learn about traffic characterization using linearly bounded arrival processes (LBAP), (o, p) regulators, leaky bucket algorithm, and packet scheduling algorithms for guaranteed service connections.
5. Study IP address lookup challenges, packet classification algorithms, flow identification methods, admission control in the Internet, differentiated services (DiffServ) architecture, and IP switching with MPLS.

Syllabus:

Unit	Topics	Lectures
I	Overview of Internet-Concepts, challenges and history. Overview of high speed networks-ATM. TCP/IP Congestion and Flow Control in Internet-Throughput analysis of TCP congestion control. TCP for high bandwidth delay networks. Fairness issues in TCP. Real Time Communications over Internet. Adaptive applications. Latency and throughput issues. Integrated Services Model (intServ). Resource reservation in Internet. RSVP.	8
II	Characterization of Traffic by Linearly Bounded arrival Processes (LBAP). Concept of (o,, p) regulator. Leaky bucket algorithm and its properties. Packet Scheduling Algorithms-requirements and choices. Scheduling guaranteed service connections. GPS, WFQ and Rate proportional algorithms. High speed scheduler design. Theory of Latency Rate servers and delay bounds in packet switched networks for LBAP traffic.	8
III	Active Queue Management - RED, WRED and Virtual clock. Control theoretic analysis of active queue management. IP address lookup-challenges. Packet classification algorithms and Flow Identification- Grid of Tries, Cross producting and controlled prefix expansion algorithms.	8
IV	Admission control in Internet. Concept of Effective bandwidth. Measurement based admission control. Differentiated Services in Internet (DiffServ). DiffServ architecture and framework.	8
V	IP switching and MPLS-Overview of IP over ATM and its evolution to IP switching. MPLS architecture and framework. MPLS Protocols. Traffic engineering issues in MPLS. [P control of Optical Routers. Lamda Switching, DWDM Networks	8

Text/References

1. Jean Wairand and Pravin Varaiya, High Perforamnce Communications Networks, Second Edition, 2000.
2. Jean Le Boudec and Patrick Thiran, Network Calculus A Theory of Deterministic Queueing Systems for the Internet, Springer Veriag, 2001.
3. Zhang Wang, Internet Qo,5, Morgan Kaufman 2001.

Course Outcomes:

1. Upon completion of the course, students will be able to explain the concepts, challenges, and historical development of the Internet, including high-speed networks like ATM.
2. Students will be able to analyze TCP/IP congestion and flow control mechanisms, evaluate throughput, fairness, and performance for high-bandwidth delay networks.
3. Upon completion of the course, students will be able to design and analyze real-time communications applications, considering latency, throughput, and resource reservation using the integrated services model.

4. Students will be able to characterize traffic using linearly bounded arrival processes, apply (o, p) regulators and the leaky bucket algorithm, and implement packet scheduling algorithms for guaranteed service connections.
5. Upon completion of the course, students will be able to evaluate IP address lookup methods, implement packet classification algorithms, understand admission control mechanisms, analyze differentiated services architecture, and comprehend IP switching with MPLS.

MTMC 051	Algorithms for VLSI Design Automation	L: 3	T: 1	P: 0	Credits : 3

Course Objectives:

1. Understand the VLSI design cycle and the new trends in VLSI design, including physical design automation and fabrication processes.
2. Study the algorithms and techniques for VLSI design automation, including partitioning, floor planning, pin assignment, placement, global routing, detailed routing, over the cell routing, via minimization, and compaction.
3. Explore the problem formulations and classifications of algorithms for each stage of the physical design cycle, including partitioning, floor planning, pin assignment, placement, routing, and compaction.
4. Learn about the different algorithmic approaches used in VLSI design automation, such as group migration, simulated annealing, constraint-based algorithms, simulation-based algorithms, Steiner tree-based algorithms, and hierarchical compaction.
5. Gain practical knowledge of VLSI design automation tools and understand their application in the physical design cycle.

Syllabus:

Unit	Topics	Lectures
I	**VLSI physical design automation and Fabrication** VLSI Design cycle, New trends in VLSI design, Physical design cycle, Design style, Introduction to fabrication process, design rules, layout of basic devices	8
II	**VLSI automation Algorithms Partitioning:** Problem formulation, classification ofpartitioning algorithms, Group migration algorithms, simulated annealing.	8
III	**Floor planning & pin assignment:** Problem formulation, classification of floorplanning algorithms, constraint based floor planning, floor planning algorithms for mixedblock& cell design, chip planning, pin assignment, problem formulation, classificationof pin assignment algorithms, General & channel pin assignment Placement Problemformulation, classification of placement algorithms, simulation base placementalgorithms, recent trends in placement	8
IV	**Global Routing and Detailed routing:** Problem formulation, classification of global routingalgorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms,performance driven routing Detailed routing problem formulation, classification ofrouting algorithms, introduction to single layer routing algorithms, two layer channelrouting algorithms, greedy channel routing, switchbox routing algorithms.	8
V	**Over the cell routing & via minimization:** Two layers over the cell routers,constrained & unconstrained via minimization **Compaction:** Problem formulation, classification of compaction algorithms, onedimensionalcompaction, two dimension based compaction, hierarchical compaction	8

Reference Books :

1. NaveedShervani, “Algorithms for VLSI physical design Automation”, KluwerAcademic Publisher, Second edition.
2. ChristophnMeinel& Thorsten Theobold, “Algorithm and Data Structures for VLSIDesign”, Kluwer Academic Publisher.
3. R. Drechsler, “Evolutionary Algorithm for VLSI CAD”, Kluwer Academic Publication.

Course Outcomes:

1. Upon completion of the course, students will be able to explain the VLSI design cycle and the current trends in VLSI design, including physical design automation and fabrication processes.
2. Students will be able to analyze and apply partitioning algorithms for efficient VLSI design, considering problem formulations and classifications.
3. Upon completion of the course, students will be able to design floor plans and assign pins using constraint-based algorithms and analyze the algorithms used for mixed block and cell design.
4. Students will be able to implement placement algorithms for effective VLSI design, considering problem formulations and classifications, and understand the recent trends in placement techniques.
5. Upon completion of the course, students will be able to design global and detailed routing solutions, implement over the cell routing techniques, minimize vias, and perform compaction using appropriate algorithms.

MTMC 052	MEMS & Micro Sensor Design	L: 3	T: 1	P: 0	Credits : 3

Course Objectives:

1. Understand the fundamentals of MEMS (Microelectromechanical Systems) and their applications in various fields.
2. Study the fabrication technologies and processes used in MEMS, including micromachining techniques and materials selection.
3. Explore the mechanics of beam and diaphragm structures, including stress, strain, Hooke's Law, bending moment, and displacement.
4. Learn about air damping and its effects on micro-dynamics, including drag effects, squeeze-film air damping, and slide-film air damping.
5. Study the principles of electrostatic actuation, including electrostatic forces, fringe effects, and driving mechanisms for mechanical actuators.

Syllabus:

Unit	Topics	Lectures
I	Introduction to MEMS, MEMS Fabrication Technologies, Materials and Substrates for MEMS, Processes forMicromachining, Characteristics, Sensors/Transducers, Piezoresistance Effect,Piezoelectricity, Piezoresistive Sensor.	8
II	**Mechanics of Beam and Diaphragm Structures**,Stress and Strain, Hooke's Law. Stress and Strain of Beam Structures: Stress, Strain in aBent Beam, Bending Moment and the Moment of Inertia, Displacement of BeamStructures Under Weight, Bending of Cantilever Beam Under Weight.	8
III	**Air Damping**,Drag Effect of a Fluid: Viscosity of a Fluid, Viscous Flow of a Fluid, Drag ForceDamping, The Effects of Air Damping on Micro-Dynamics. Squeeze-film Air Damping:Reynolds' Equations for Squeeze-film Air Damping, Damping of Perforated ThickPlates. Slide-film Air Damping: Basic Equations for Slide-film Air Damping,Couette-flow Model, Stokes-flow Model.	8
IV	**Electrostatic Actuation** Electrostatic Forces, Normal Force, Tangential Force, Fringe Effects, ElectrostaticDriving of Mechanical Actuators: Parallel -plate Actuator, Capacitive sensors. Step and Alternative Voltage Driving: Step Voltage Driving, Negative SpringEffect and Vibration Frequency.	8
V	**Thermal Effects**, Temperature coefficient of resistance, Thermo-electricity, Thermocouples, Thermal andtemperature sensors. **Applications of MEMS in RF**,MEMS Resonator Design Considerations, One-Port Micromechanical ResonatorModeling Vertical Displacement Two-Port Microresonator Modeling,Micromechanical Resonator Limitations.	8

Reference Books:

1. S.M. Sze, “Semiconductor Sensors”, John Wiley & Sons Inc., Wiley Interscience Pub.
2. M.J. Usher, “Sensors and Transducers”, McMillian Hampshire.
3. RS Muller, Howe, Senturia and Smith, “Micro sensors”, IEEE Press.

Course Outcomes:

1. Upon completion of the course, students will be able to explain the concepts and applications of MEMS in various fields, such as sensors, transducers, and RF devices.
2. Students will be able to analyze and apply different fabrication technologies and processes used in MEMS, considering materials selection and micromachining techniques.

3. Upon completion of the course, students will be able to calculate stress, strain, bending moment, and displacement in beam and diaphragm structures.
4. Students will be able to analyze the effects of air damping on micro-dynamics, including drag effects and various models of squeeze-film and slide-film air damping.
5. Upon completion of the course, students will be able to analyze electrostatic actuation principles, calculate electrostatic forces, and understand the driving mechanisms for mechanical actuators.

MTMC 053	Embedded System for Wireless & Mobile Communication	L: 3	T: 1	P: 0	Credits : 3

Course Objective: After completion of this course student will be able to:

1. Understand the importance of embedded systems, it components, peripherals and requirements.
2. Knowledge about hardware and software co-design used in microcontrollers and their issues and trade-offs.
3. Knowledge about the Wireless technologies.
4. Knowledge about the Bluetooth protocols and communication using Bluetooth.
5. Knowledge about the Bluetooth networking, connection establishment procedure, Bluetooth security architecture and its levels.
6. Knowledge about the java programming J2ME architecture and packages.
7. Understand the working Bluetooth client and server application, JINI, IrDA, Wireless LAN.

Syllabus:

Unit	Topics	Lectures
I	**Typical Embedded System:** Core of the Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware, Other System Components.	8
II	**Characteristics and Quality Attributes of Embedded Systems:** Hardware Software Co-Design and Program Modeling: Fundamental Issues in Hardware Software Co-Design, Computational Models in Embedded Design, Introduction to Unified Modeling Language, Hardware Software Trade-offs.Introduction to wireless technologies: WAP services, Serial and Parallel Communication, Asynchronous and synchronous Communication, FDM,TDM, TFM, Spread spectrum technology	8
III	Introduction to Bluetooth: Specification, Core protocols, Cable replacement protocol Bluetooth Radio: Type of Antenna, Antenna Parameters, Frequency hoping Bluetooth Networking: Wireless networking, wireless network types, devices roles and states, adhoc network, scatter net Connection establishment procedure, notable aspects of connection establishment, Mode of connection, Bluetooth security, Security architecture, Security level of services, Profile and usage model: Generic access profile (GAP), SDA, Serial port profile,	8
IV	Secondary Bluetooth profile Hardware: Bluetooth Implementation, Baseband overview, packet format, Transmission buffers, Protocol Implementation: Link Manager Protocol, Logical Link Control Adaptation Protocol, Host control Interface, Protocol Interaction with layers	8
V	Programming with Java: Java Programming, J2ME architecture, Javax. Bluetooth package Interface, classes, exceptions, Javax. obex Package: interfaces, classes Bluetooth services registration and search application, Bluetooth client and server application. Overview of IrDA, Home RF, Wireless LANs, JINI	8

Reference Books:

1. hibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Ltd

1. C.S.R. Prabhu and A.P. Reddi," Bluetooth Technology", PHI Publication.
2. U. Dalal& M. Shukla, "Wireless & Mobile Communication", Oxford University Press.
3. C. Y. William, Lee, "Mobile communication engineering theory and applications", TMH, Publication.
4. S .Haykins, "Communication Systems", John Wiley and Sons.

Course Outcomes:

CO053.1	To develop the understanding of the importance of embedded systems, its components, peripherals and requirements.
CO053.2	Understanding of about hardware and software co-design used in microcontrollers and their issues and trade-offs
CO053.3	Understanding about the Wireless technologies, types of digital communications that can be used in microcontroller.
CO053.4	To understand the Bluetooth protocols and communication using Bluetooth Radio antenna and its types
CO053.5	To understand about the Bluetooth networking, connection establishment procedure, Bluetooth security architecture and its levels
CO053.6	To understand the Secondary Bluetooth profile, packet format, protocol implementation: L2CAP, host control, link control
CO053.7	To understand about the java programming J2ME architecture and packages
CO053.8	To understand the Bluetooth client and server application, JINI, IrDA, Wireless LAN

MTMC 054	Artificial Neural Networks	L: 3	T: 1	P: 0	Credits : 3

Course Objective: After completion of this course student will be able to:

1. Understand the basics of artificial neural network
2. Comprehend architecture of supervised and unsupervised learning
3. Implement the training and testing algorithms of supervised learning
4. Describe associated models
5. Apply the knowledge to develop solution of various problems by implementing optimization techniques.

Syllabus:

Unit	Topics	Lectures
I	Introduction: Biological neurons and memory: Structure and function of a single neuron; Artificial Neural Networks (ANN); Typical applications of ANNs : Classification, Clustering, Vector Quantization, Pattern Recognition, Function Approximation, Forecasting, Control, Optimization; Basic Approach of the working of ANN - Training, Learning and Generalization.	8
II	Supervised Learning: Single-layer networks; Perceptron-Linear separability, Training algorithm, Limitations; Multi-layer networks-Architecture, Back Propagation Algorithm (BTA) and other training algorithms, Applications. Adaptive Multi-layer networks-Architecture, training algorithms; Recurrent Networks; Feed-forward networks; Radial-Basis-Function (RBF) networks.	8
III	Unsupervised Learning: Winner-takes-all networks; Hamming networks; Maxnet; Simple competitive learning; Vector-Quantization; Counter propagation networks; Adaptive Resonance Theory; Kohonen's Self-organizing Maps; Principal Component Analysis.	8
IV	Associated Models: Hopfield Networks, Brain-in-a-Box network; Boltzmann machine.	8
V	Optimization Methods: Hopfield Networks for-TSP, Solution of simultaneous linear equations; Iterated Gradient Descent; Simulated Annealing; Genetic Algorithm.	8

Texts/References

1. K. Mehrotra, C.K. Mohan and Sanjay Ranka, Elements of Artificial Neural Networks, MIT Press, 1997 - [Indian Reprint Penram International Publishing (India), 1997]
2. Simon Haykin, Neural Networks - A Comprehensive Foundation, Macmillan Publishing Co., New York, 1994.
3. A Cichocki and R. Unbehauen, Neural Networks for Optimization and Signal Processing, John Wiley and Sons, 1993.
4. J. M. Zurada, Introduction to Artificial Neural Networks, (Indian edition) Jaico Publishers, Mumbai, 1997.

Course Outcomes:

CO054.1	Introduction of artificial neural network
CO054.2	Architecture and training algorithms of supervised learning
CO054.3	Models of unsupervised learning
CO054.4	Boltzmann machine, brain-in-a-box network, Hopfield network
CO054.5	Various networks used as Optimization method